Studies of protection resistor and HV decoupling capacitor values on MGPA output pulse shape.

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Test system

A schematic view of the system used for the studies is shown in figure 1. An HV card was modified to allow the insertion of a resistor (or a shorting wire link) in either location 1 or 2, either side of the HV decoupling capacitor Cdec. A test signal was injected at the point where the VPT anode was connected (note that the VPT was left connected, unbiased, so that any effect of its associated capacitance would not be neglected). A 50 cm long thin coax cable linked the HV card to the mothercard on which the VFE card was mounted. The output signals of the MGPA were monitored directly using a differential probe. The aim was to represent the system in a way that matches the final arrangement as closely as possible.

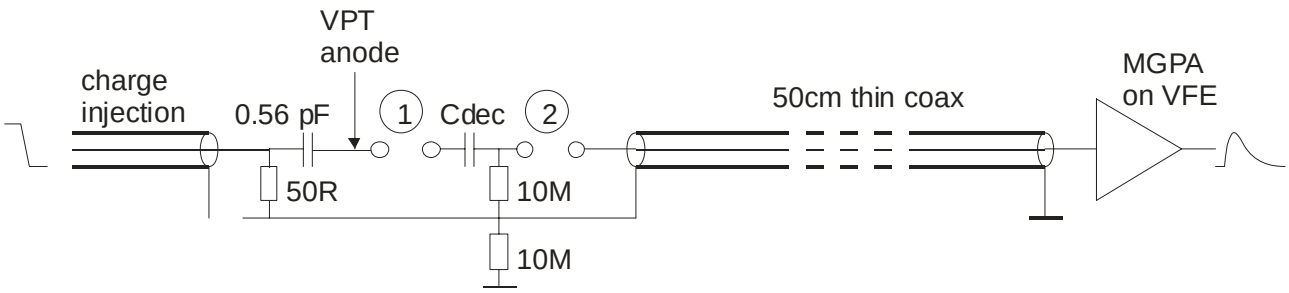

Figure 1. Schematic view of the test system

Results

Figure 2 shows the effect of different values of the HV decoupling capacitor on the signal size, varying the value from the original 1 nF through the new preferred value of 470 pF, including results for values as low as 270 and 150 pF. The reductions in pulse height are consistent with a total capacitance (including the charge injection capacitor) of ~18 pF associated with the VPT anode. Figure 1 demonstrates that Cdec can be chosen to be quite small if the capacitance at the anode side of Cdec is also small, possibly even less than the currently preferred value of 470 pF.

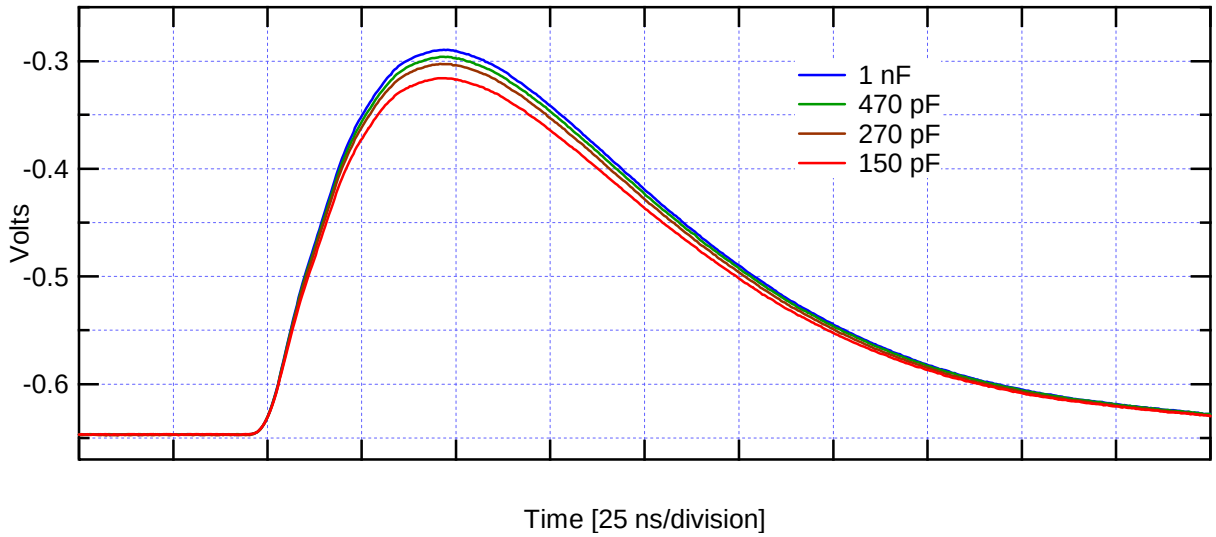

Figure 2. Effect of HV decoupling capacitor Cdec on pulse amplitude. Shorting wire links in resistor positions 1 and 2.

Figure 3 shows the effect on the pulse shape of adding resistance in location 1 in figure 1, between the VPT anode connection and Cdec, in this case for Cdec = 1nF. Figure 4 shows the same picture, but this time for resistance in location 2, after the decoupling capacitor at the input of the coaxial cable. The effect on the pulse shape is more significant for location 2, because of the additional capacitance to the left of the added resistor, associated with the pcb tracks and the decoupling capacitor itself

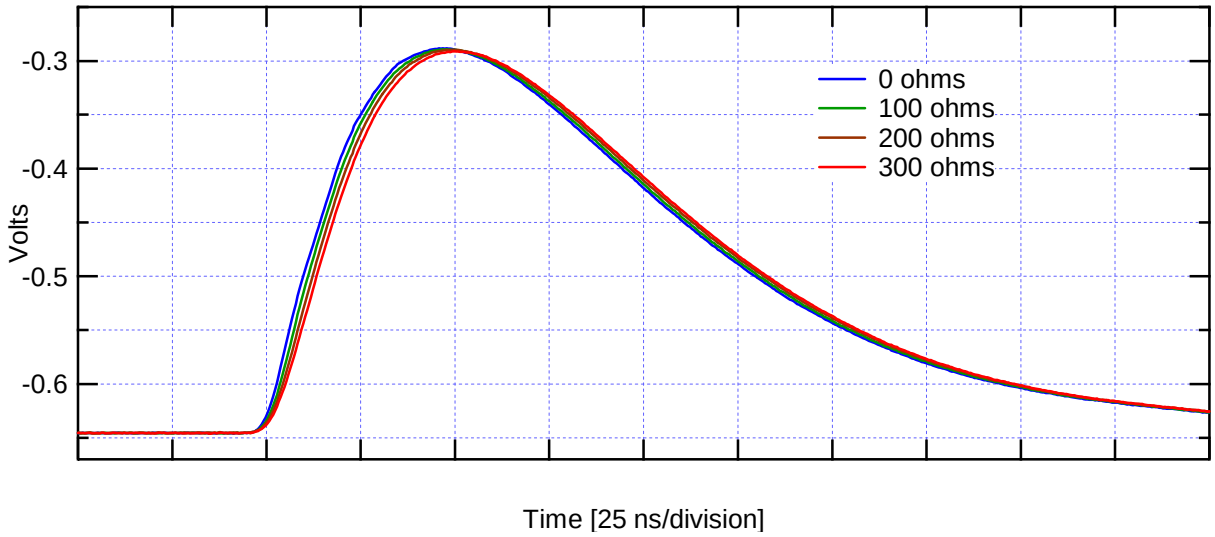

Figure 3. Effect on pulse shape of adding resistance in location 1, for Cdec = 1nF

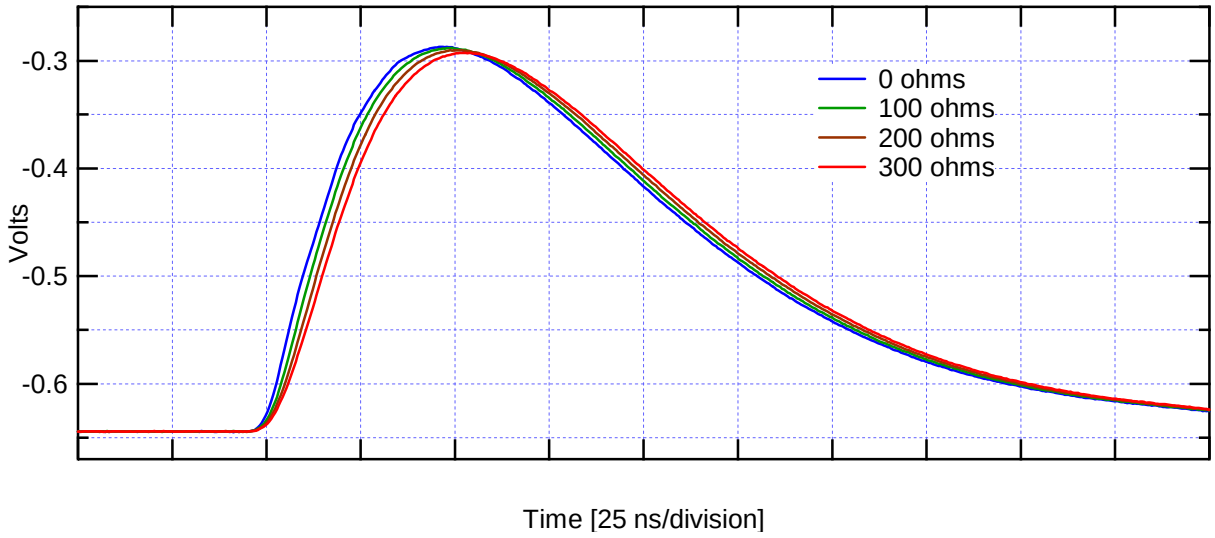

Figure 4. Effect on pulse shape of adding resistance in location 2, for Cdec = 1nF

Figures 5 and 6, 7 and 8, and 8 and 9 show the equivalent pictures to figures 3 and 4, but for values for Cdec of 470 pF, 270 pF and 150 pF respectively.

Cdec = 470 pF.

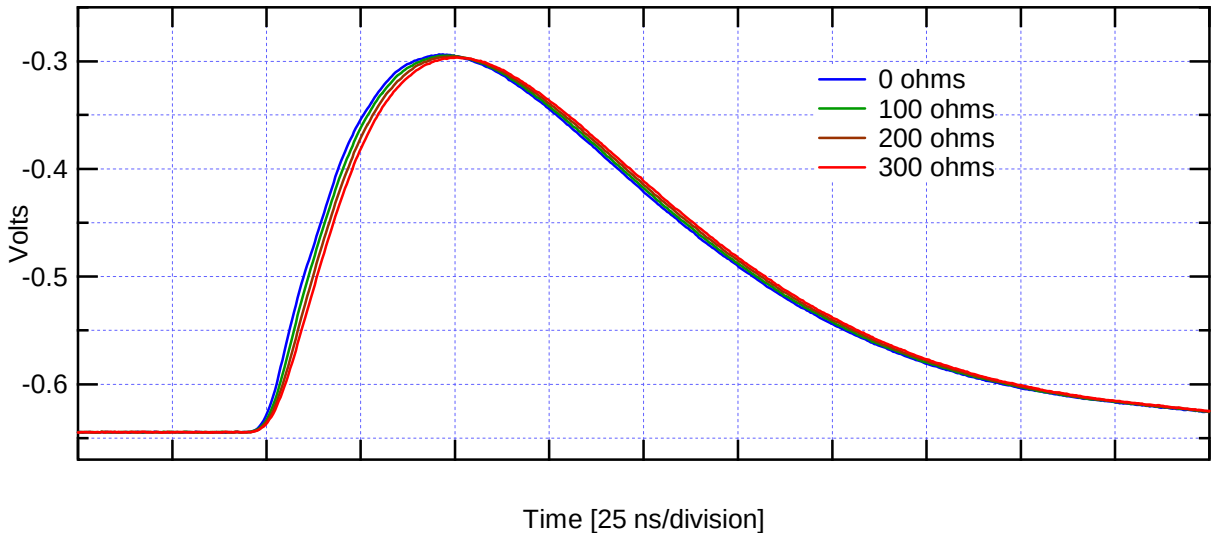

Figure 5. Effect on pulse shape of adding resistance in location 1, for Cdec = 470 pF

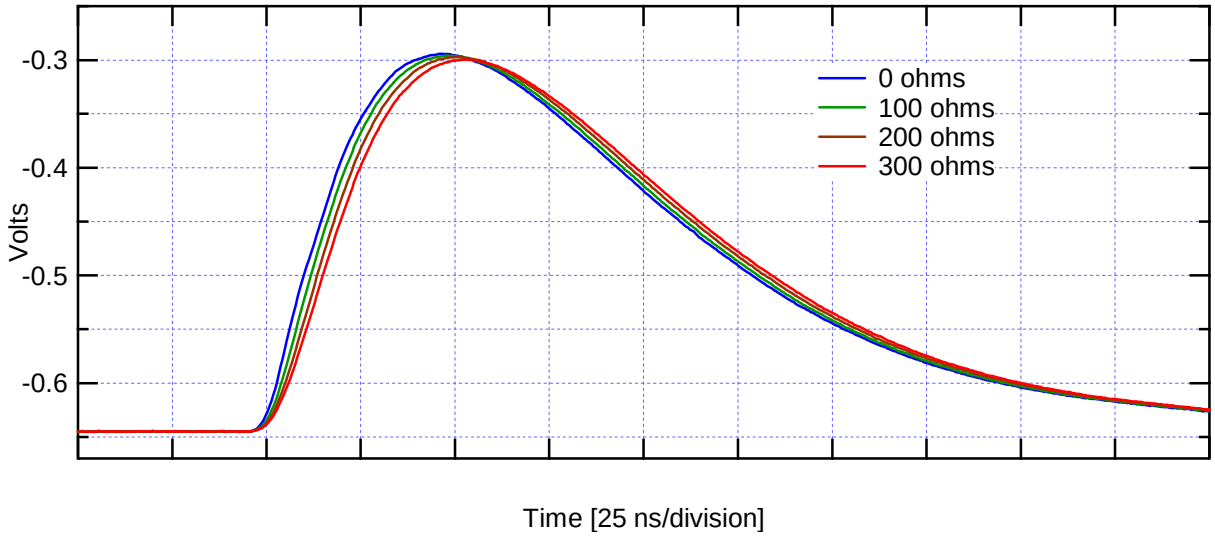

Figure 6. Effect on pulse shape of adding resistance in location 2, for Cdec = 470 pF

Cdec = 270 pF.

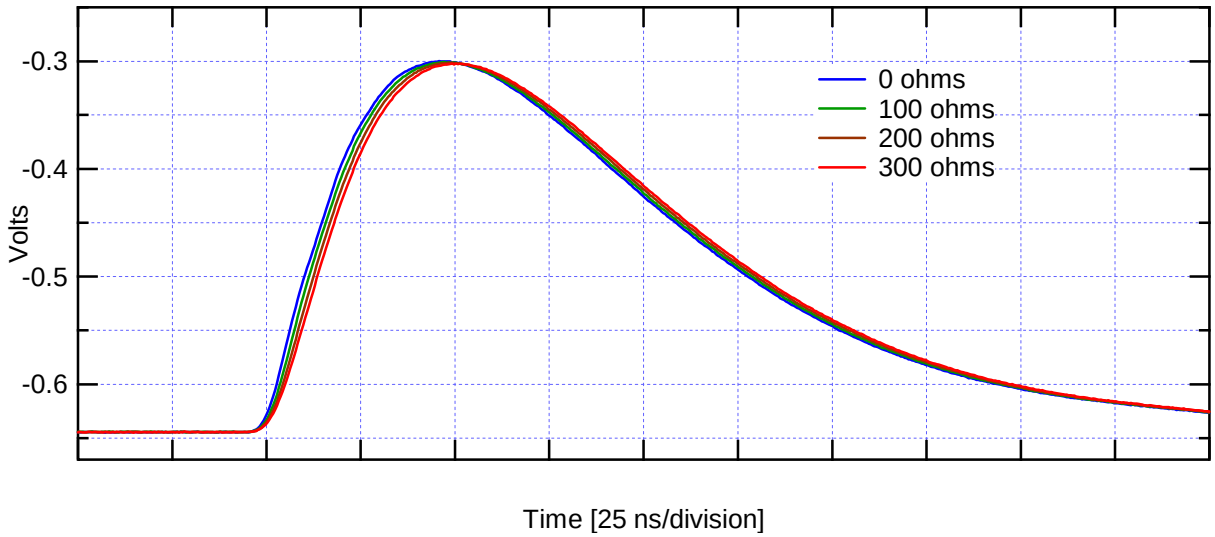

Figure 7. Effect on pulse shape of adding resistance in location 1, for Cdec = 270 pF

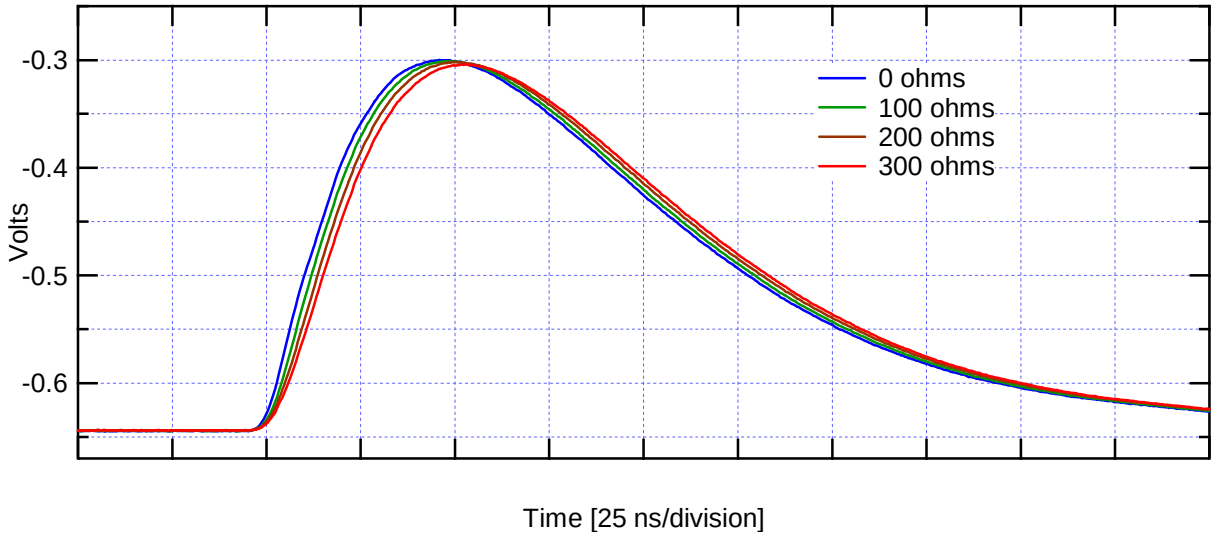

Figure 8. Effect on pulse shape of adding resistance in location 2, for Cdec = 270 pF

Cdec = 150 pF.

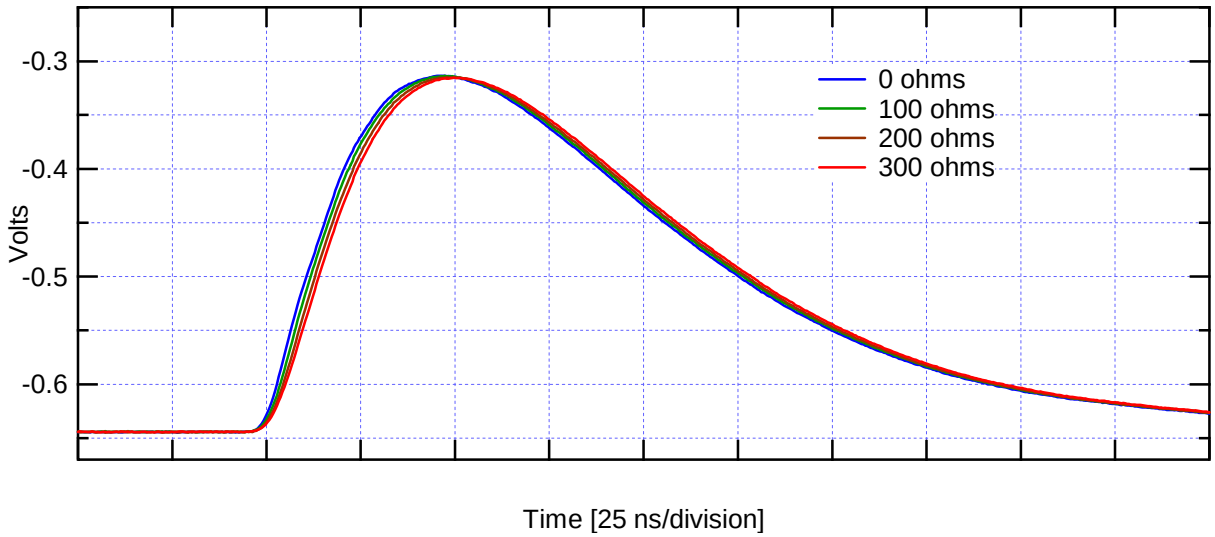

Figure 9. Effect on pulse shape of adding resistance in location 1, for Cdec = 150 pF

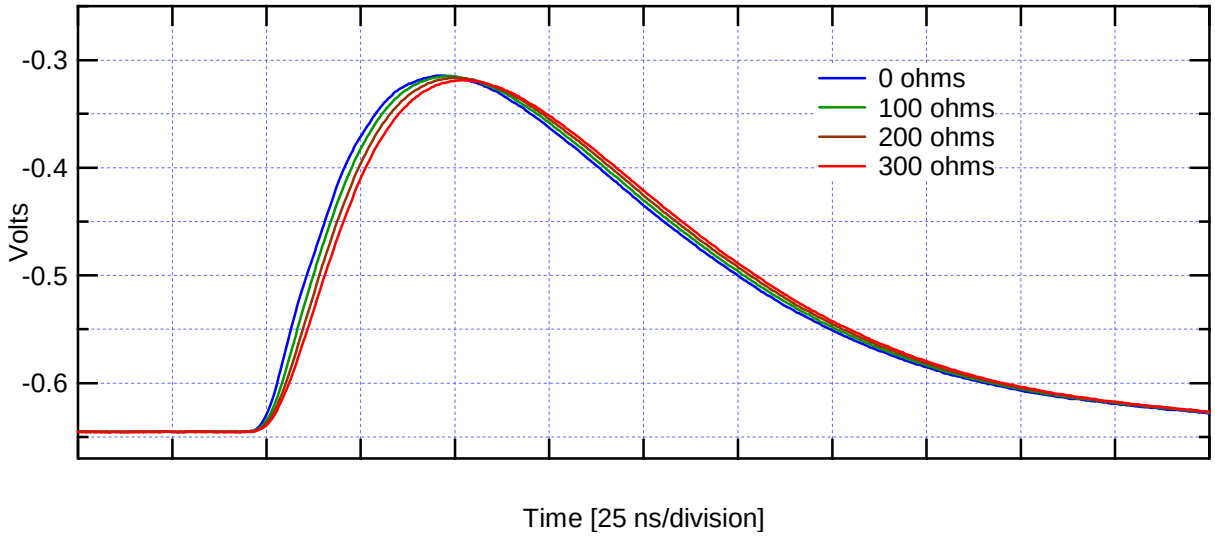

Figure 10. Effect on pulse shape of adding resistance in location 2, for Cdec = 150 pF

Discussion and conclusions

To minimise the risk of damage to the MGPA due to VPT breakdown it is desirable to minimise the value of Cdec, and to include a series resistor, with as large a value as possible. Figure 1 indicates that there may be scope for reducing Cdec still further from its current choice of 470 pF, if necessary. Note that the value of ~18 pF deduced for the capacitance associated with the VPT anode is comparable with but slightly less than the 30 pF reported from previous measurements at RAL

Comparing the pairs of figures for the different locations of the series resistor for each value of Cdec it is clear that the effect of the resistance on the pulse shape is independent of the value of Cdec. It is also clear that location 1 is preferred if we want to maximise the resistor value and minimise the effect on the pulse shape. Examining the pulse shapes the peaking time increases by ~ 1 ns / 100 Ω added resistance for location 1 and ~ 2 ns / 100 Ω added resistance for location 2. For example the pulse peaking time increases by 6 ns for a 300 Ω added resistance in location 2, but only 3 ns for the same resistor in location 1.

The effect of the resistor is to slow down the discharge path to the MGPA input of any capacitance to its left in figure 1, which is why it is preferable to put it as close to the VPT anode as possible. For a value of 100 Ω the effect is negligible, and either location could be used, but if we did want to choose a larger value, to increase the protection margin, it should probably go in location 1. I understand that this is more difficult from the viewpoint of the HV card layout.

I think it is reasonable to conclude that a 100 Ω series resistor could go either side of the HV decoupling capacitor without significantly affecting the pulse shape.