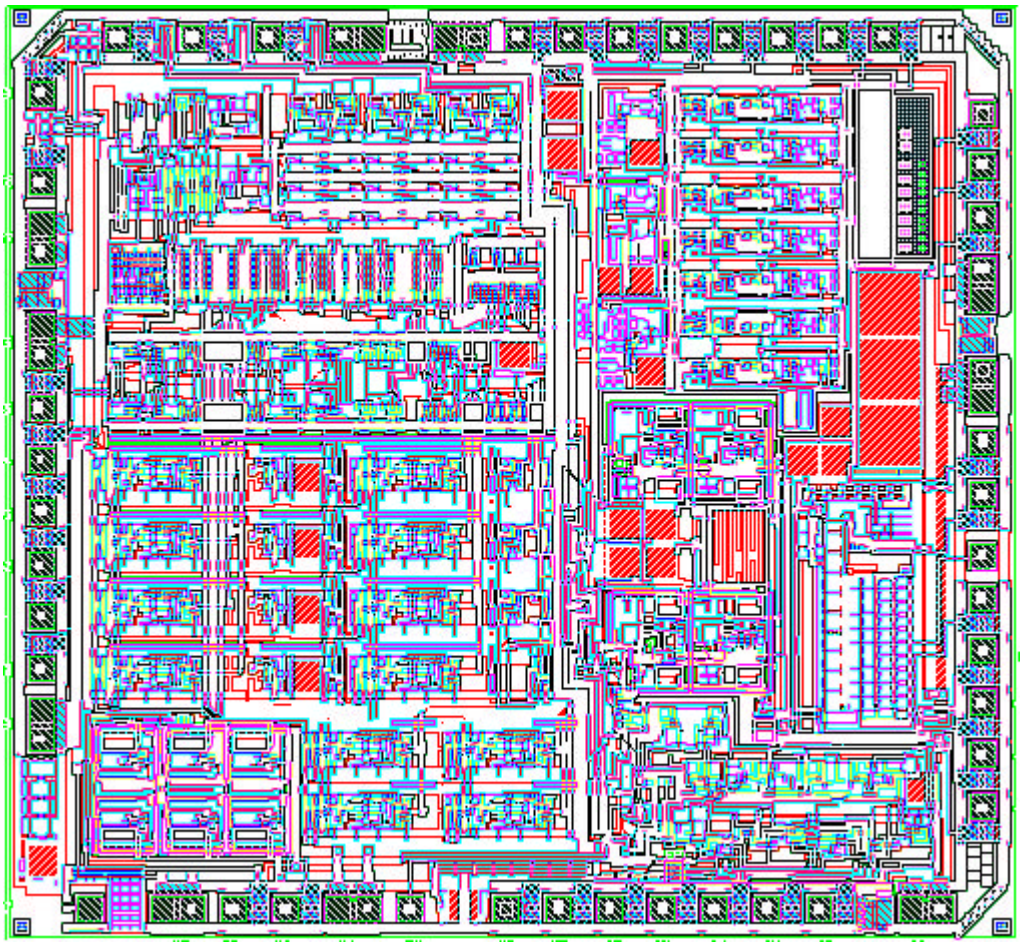
FPPA Specification Document



FEATURES

Version 1.2
Last version : FPPA2000.
ECAL Barrel specifications (from simulation).

FPPA Specification Document

FPPA Design Team	
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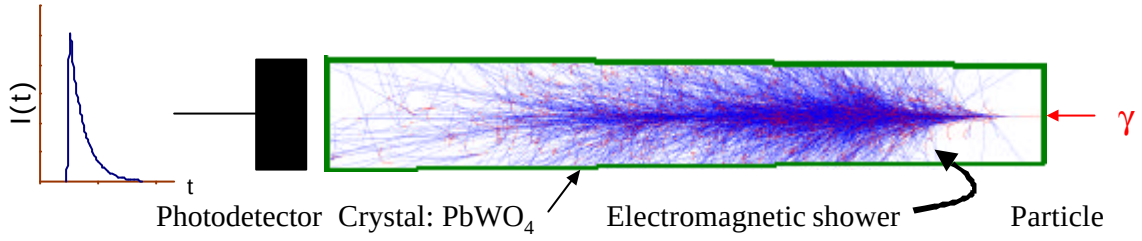
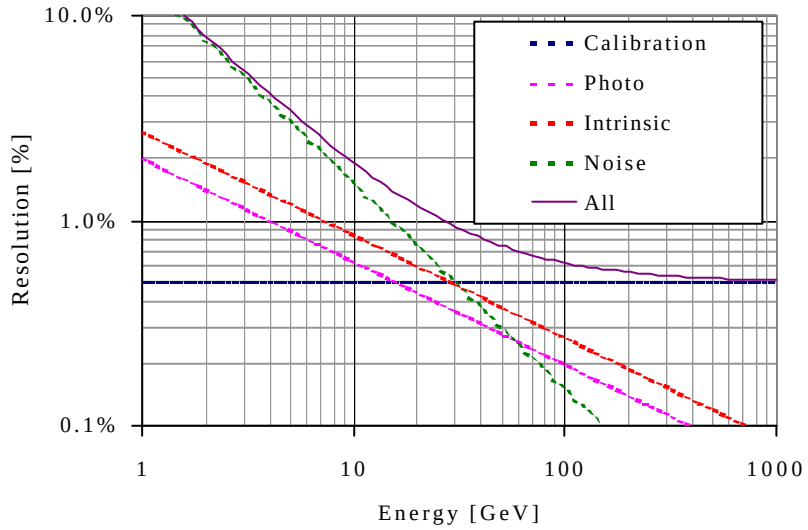
1. INTRODUCTION

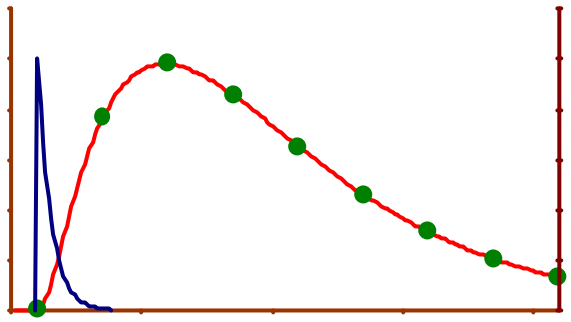
The CMS Electromagnetic Calorimeter (***ECAL***) will consist of ~80 000 scintillating crystals. Electromagnetically interacting particles create scintillation light in the crystals proportional to their energy. By measuring the amount of light, and knowing the crystal's location, the energy and position of the particle may be reconstructed. The interactions occur every ***bunch crossing***. The amount of energy deposited in a given crystal during a given bunch crossing is unrelated to the amount deposited during previous or subsequent bunch crossings.
A photodetector converts the scintillation light into a photocurrent. In the ***barrel*** part of the ECAL (the central cylinder of crystals), each crystal is equipped with two 25mm^2 silicon avalanche photodiodes (***APD***). The reverse-biased APD cathodes are connected together to sum the current. In the ***endcaps*** (the two disks of crystals at the ends of the cylindrical barrel), vacuum phototetrodes (***VPT***) are used.



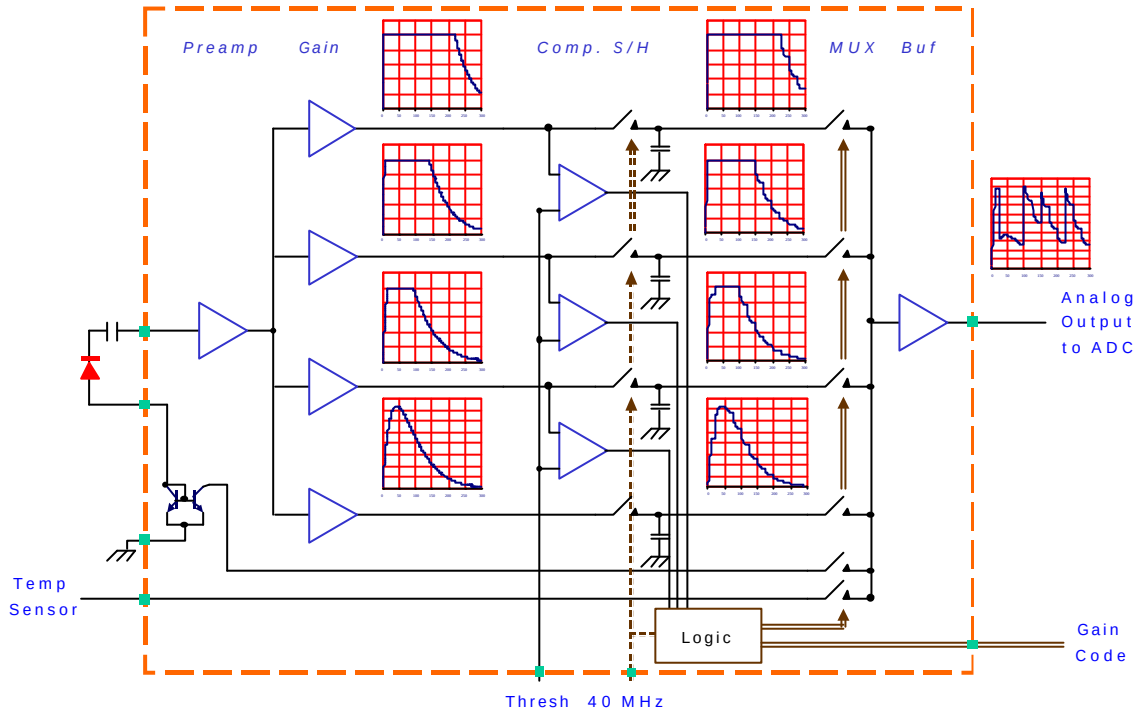
1.2. DESIGN CRITERIA



The ECAL requires a wide dynamic range, low noise readout in order to achieve its physics goals. The key design parameter is ***energy resolution***, which represents the precision with which particle energies are reconstructed. The energy resolution is the width of a histogram of reconstructed energy of particles of energy E from all locations in the calorimeter, divided by E. As shown in the graph, the resolution has several components. Intrinsic represents fluctuations in energy containment of the crystals. Photo represents the gaussian statistics in the number of photons produced (along with the excess noise factor of the photodetector). Noise is the contribution from electronic noise. Note that several crystals must be added together to reconstruct the energy, so that the noise per channel is lower than that shown in the graph. In addition, as channels must be added, correlated noise must be kept to a minimum. Calibration represents our ability to maintain the energy calibration of all crystals across the detector. It also includes all residual electronic non-linearity or errors.

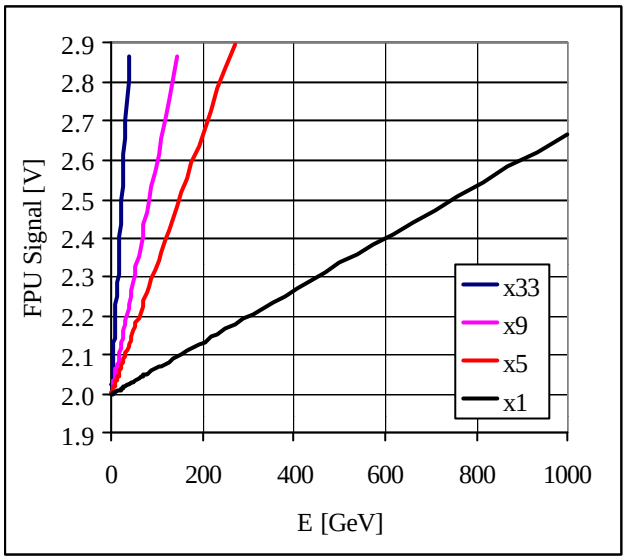


PbWO4 is a relatively fast scintillator, with a principle decay time constant of 10 ns. We have chosen to make a voltage-sampling system running at the LHC collision frequency of 40 MHz. From a noise point of view, a long signal shaping time would be ideal. Due to the high background rate at the LHC, however, long shaping times add pileup noise. We have thus chosen 40 ns double integration (δ-function response $\frac{t}{t}e^{-t/t}$). The data collected for a given pulse are thus the dots shown above : the fast curve represents the scintillation light, the slower curve represents the shaped pulse being sampled, and the dots are the stored voltage samples. Via these samples, the amplitude - and hence energy - and timing of the incident pulse may be reconstructed.



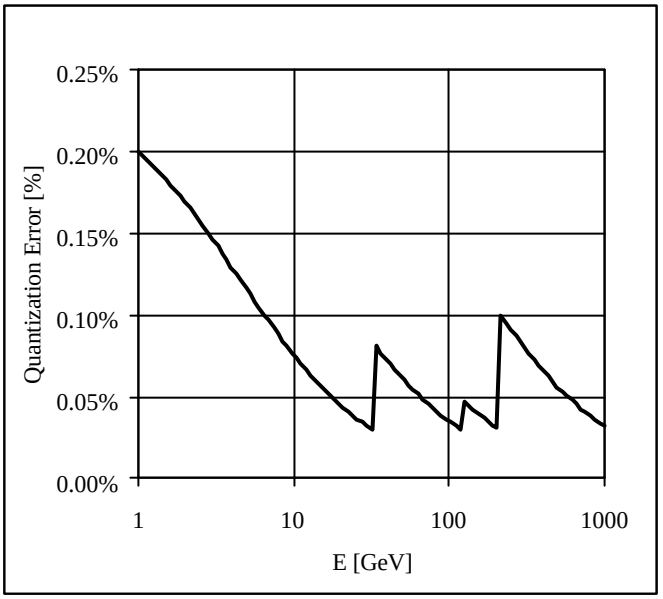
In order to achieve the best performance, the signal acquisition and conversion electronics are mounted directly behind the crystals in the CMS detector. This sets constraints on the total power consumption, and on radiation hardness requirements, as the maximum dose in the barrel part of the detector is 1 MRad along with $2x10^{13}$ n/cm^2 (1 MeV equivalent) over the 10-year detector lifetime. Doses rise in the endcap region, and we will limit the placement of electronics such that the maximum lifetime radiation requirement is 2.5 MRad along with $5x10^{13}$ n/cm^2.

The figure above shows the basic acquisition scheme. The preamplifier is AC-coupled to the APD cathode (the APD is reverse-biased). Following the preamplifier are four gain stages, with gains 1, 5, 9 and 33. The gain stages have clamps to prevent saturation. The Floating Point Unit, which selects the gains and multiplexes them to an ADC, follows the gain stages. The FPU consists of a series of analog switches, comparators and digital logic. Directly after the gain, analog switches are used to form a sample/hold amplifier. Comparators on the three highest gain stages along with digital logic determine which gain stage has the largest, non-saturated signal and multiplex that signal to the ADC via the output buffer. The digital logic also outputs a code indicating which gain range was used.

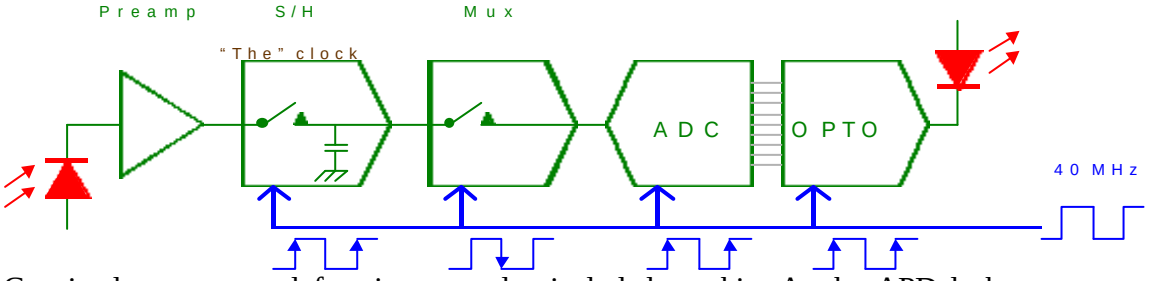


The gains have the form $1+R_2/R_1$ and the bandwidth, which should be the same for all gain stages, is of the form R_2C. For optimal matching, the different R_2 and C are formed by unit elements: $R_2 = nr$ and $C = mc$, hence we arrive at 1,5,9 and 33. As a function of energy (in the barrel) the FPU signal output (1.9 to 2.9V - to match the AD9042 ADC input) - is shown at left (assuming a 100 mV pedestal level). The comparator threshold is set at 80% of full-scale (i.e. for the plot shown on the left, the range changes once the signal reaches 800 mV).

A major design goal for the electronics is that it should not degrade the intrinsic energy resolution. With the multi-range scheme above, the contribution from the 12-bit ADC quantization error is given by the curve on the right. Here, the quantization error has been conservatively taken as $1/N$ rather than $1/\sqrt{12}N$, where N is the value of the ADC output code. The design target is to keep the error less than 0.1% for energies greater than around 20 GeV.



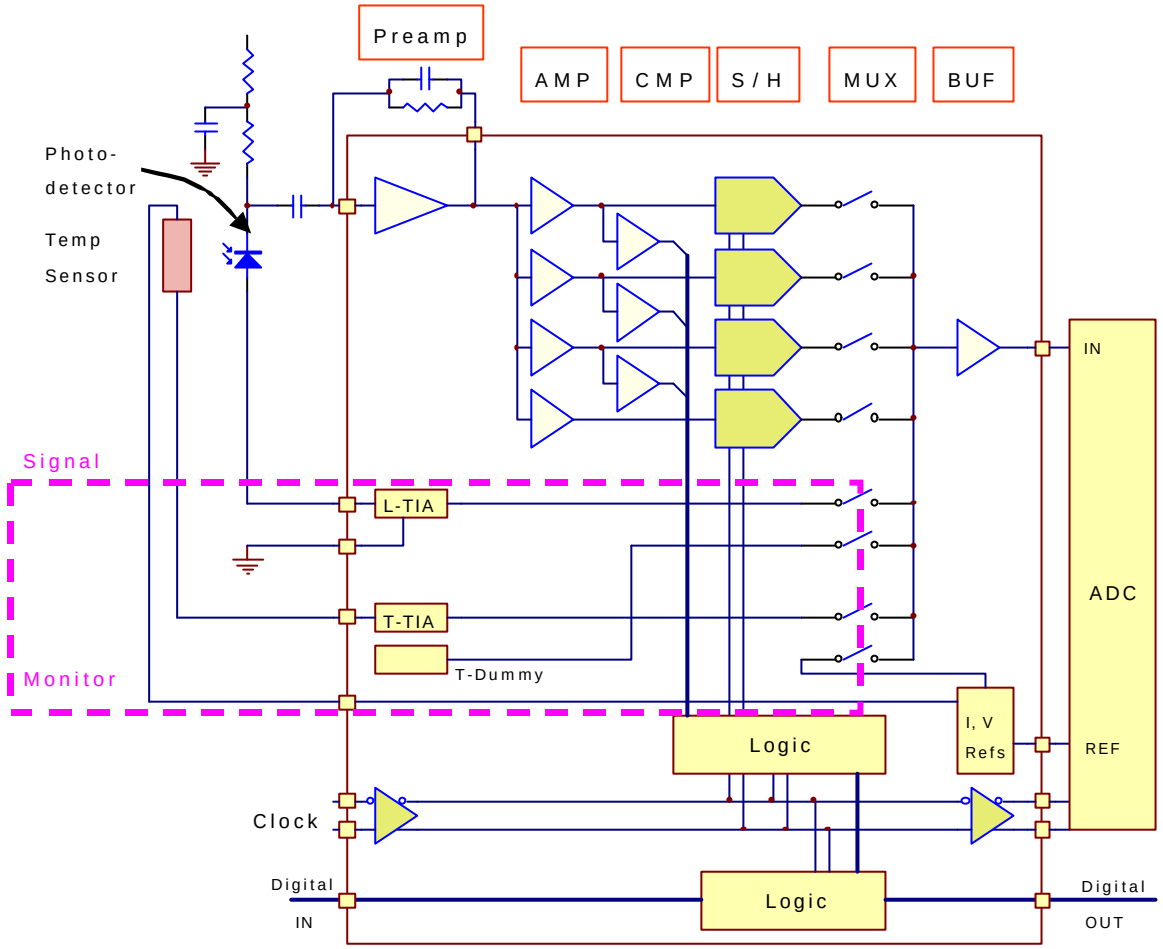
The complete readout channel consists of the FPPA followed by a commercial ADC (Analog Devices AD9042) and a custom optical link. One clock is used to control the three chips: The leading edge of the clock controls the S/H. The falling edge registers the multiplexers, and the ADC encodes on the rising edge. The ADC includes an internal S/H, so that with the ADC acquisition time, as well as the transit time through the FPU, the ADC encodes the held level roughly 1ns before the S/H switches back to track mode. The FPU includes three pipeline delays on the output bit in order to match the ADC latency.



Certain detector control functions are also included on-chip. As the APD leakage current increases with neutron fluence, the APD leakage current is monitored via the anode. In addition, both the crystal and APD are temperature sensitive, so circuitry to multiplex a temperature sensor to the ADC is also included.

2. BLOCK DIAGRAM

The FPPA consists of two primary functional blocks:
The ***Signal*** block contains all of the circuitry needed to acquire and condition the detector signal. The ***Monitor*** block contains additional circuitry used to monitor the state of the detector (APD leakage current and APD+crystal temperature).



2.2. PREAMPLIFIER

The preamplifier converts the photocurrent sensor into a voltage waveform to be sampled. Included in the preamplifier are the elements, which shape the pulse. The overall gain of the pulse is fixed primarily by the external feedback resistor and capacitor. These components, along with internal resistors, capacitors and the input transistor, determine the pulse shape.
Four gains stage follow the preamplifier, which is the only element in the FPPA covering the full dynamic range. The ratios of internal metal resistors, which have low thermal coefficients and are radiation resistant, fix gains.

2.2.1. BARREL AND ENDCAP VERSIONS

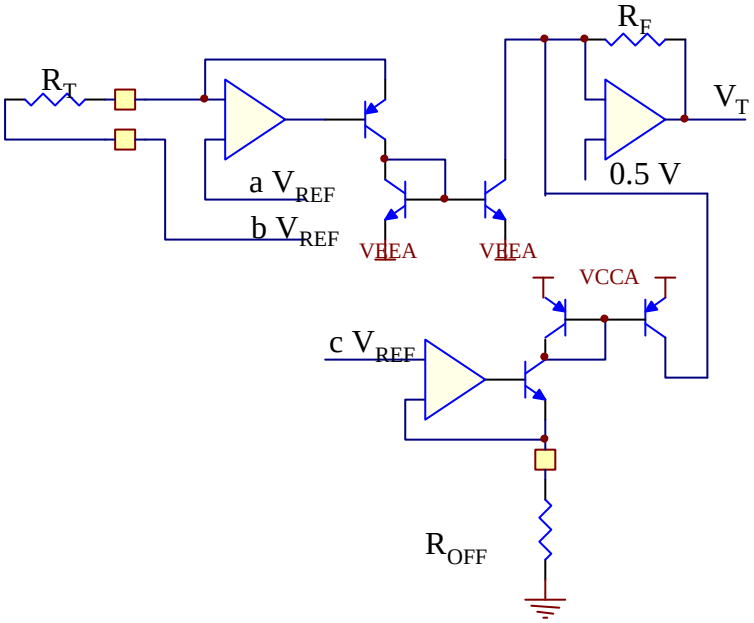
The detector capacitance figures in the expression for the noise and shaping time constants of the preamplifier. As the ***barrel*** and ***endcaps*** use different photodetectors, and have different full-scale charge, different versions are required. For simplicity, there is one layout, which can be changed from a barrel to an endcap version via a metal mask change.

2.3. FPU (FLOATING POINT UNIT)

The FPU consists of analog switches, comparators and digital logic. Sample/Hold, which stores the value of the sampled waveform, follows each gain stage. The 3 highest gain stages have comparators and digital logic, which selects the appropriate gain range - i.e. the highest gain below a fixed threshold. For normal data taking, the FPU operates in *auto* mode - i.e. it samples the waveform as described above. In addition, in *force* mode, any of the FPU MUX switches can be selected.

2.4. TEMPERATURE AND LEAKAGE CURRENT (MONITOR)

2.4.1. TEMPERATURE MEASUREMENT



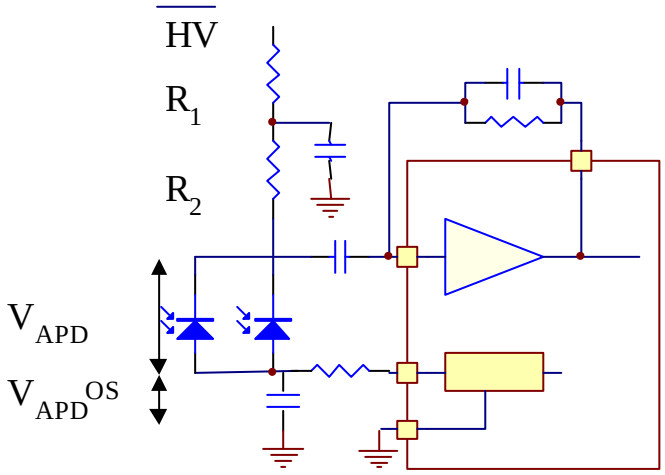
A thermistor measures temperatures. Scaled copies of the ADC buffered reference are applied to the thermistor, as shown on the left. The "temperature voltage" is

$$V_T = R_F\left[\frac{a}{R_T} - \frac{b}{R_T} + \frac{c}{R_{OFF}}\right]V_{REF}$$

where R_T is the resistance of the thermistor $R_T = Ae^{b/T}$. In order to minimize the full dynamic temperature range over the 12 bit of ADC, an offset ("0 °C") voltage is subtracted.

As the ADC reference is used to set the current, the digitized value of V_T does not change with radiation. In order to monitor possible radiation effects (in the circuit), a dummy channel (the same circuitry, but connected to an internal, metal resistor) has been provided. As the dummy channel is identical to the temperature channel, it should track any changes.

2.4.2. LEAKAGE CURRENT MEASUREMENT



During operation, displacement damage due to radiation will cause an increase in the leakage current of the APDs. This current must be measured in order to (slowly) compensate the *IR* drop across the series resistors. As the APD gain is quite voltage sensitive ($\Delta Gain/Gain = 3.6\%/V$ at a gain of 50), the accuracy of measurement of ΔIR should be at the level of ΔV_{APD}~20 mV to keep the gain error at the level of ~0.1%.

As shown on the left, the voltage that is across the APDs is

$$V_{APD} = HV - V_{APD}^{OS} - (R_1 + R_2)(I_{LEAK}^1 + I_{LEAK}^2)$$

where HV is the applied high voltage, V_{APD}^{OS} is the input voltage of the leakage current measurement stage, and I_{LEAK}^1 and I_{LEAK}^2 are the leakage currents of the two APDs.

2.4.3. VREF MEASUREMENT

The last multiplexer switch sends a copy of V_{REF} to the ADC. This allows a cross-check of any radiation damage in the V_{REF} amplifiers.

2.5. AUXILIARY FUNCTIONS

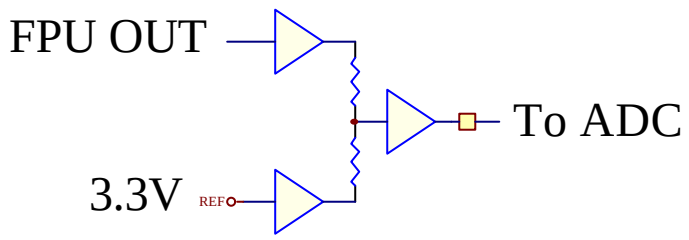
2.5.1. BIAS GENERATION

All internal bias currents and reference voltages are generated based on the 2.4V V_{REF} output of the ADC (AD9042). The AD9042 reference has a specified temperature variation of < 50 ppm/°C. Our measurements indicate a maximum gain change due to irradiation of <5 mV per LHC year, where an LHC year is defined to be 100 kRad ⊕ 10^{12} 1 MeV n/cm^2. This results in a "gain" change of 0.1% per LHC year (i.e. if 4096 ADC counts corresponded to 1.000 V at t=0, after 1 year, 4096 ADC counts correspond to 1.001 V).

2.5.2. CLOCK REGENERATOR

In order to reduce overall power consumption, the FPU regenerates the ADC clock. The clock regeneration circuit picks off the incoming PECL clock directly after it is buffered on chip. Levels are shifted to be compatible with the ADC clock input. This avoids 50Ω drivers and termination resistors for the ADC clock, as well as coupling capacitors to shift the level.

2.5.3. OUTPUT BUFFER



The output buffer drives the ADC. The ADC has a 1V signal swing, but in order to optimize noise performance, the signal swing within the chip is 2V. The output buffer must therefore divide the signal by two, add the ADC offset of 1.9V, and provide sufficient drive to charge the parasitic capacitance as well as the 2 mA ADC static load. This is accomplished by 3 essentially identical amplifiers: one creates 3.3V from the 2.4V reference; the second buffers the FPU OUTput (0.5V to 2.5V), and the third drives the ADC. The two resistors shown are equal, so the lowest voltage level output is (3.3V + 0.5V)/2 = 1.9V and the highest is (3.3V + 2.5V)/2=2.9V.

2.6. LOGIC

The static FPIN0…FPIN3 inputs program the operating mode of the FPU, as shown below. In ***Auto*** mode, the FPU runs automatically by selecting the appropriate signal range form the x1...x33 amplifiers. In ***Force*** modes, the multiplexer selects the given channel independent of the input at the preamplifier.

The multiplexer state of the FPU (i.e. which multiplexer was used on a given sample) is indicated by the FPO0 ... FPO2 outputs as shown below. In order to match the ADC latency, three clock cycles internally delay the outputs,.

The FPU does not latch FPIN0…FPIN3 inputs (as they are latched in the *CTRL* chip). Their state determines the FPU state. These bits are read back separately (via the unused 16th *SERIALIZER* bits), so that the state of the system at any time is known.

2.6.1. PROGRAMMING THE FPU STATE

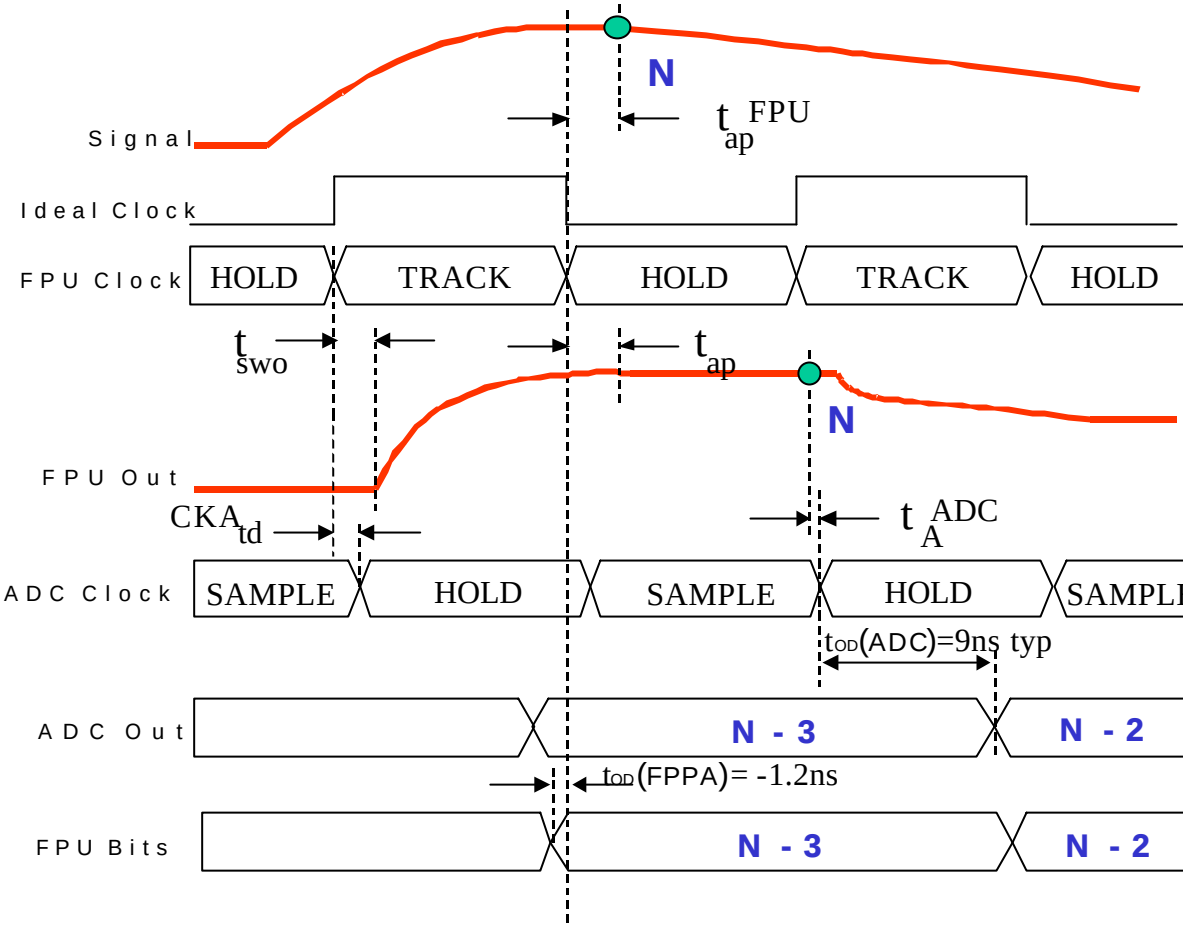
Mode	*FPIN3*	*FPIN2*	*FPIN1*	*FPIN0*
Auto	0	0	0	0
Force x33	1	0	0	0
Force x9	1	0	0	1
Force x5	1	0	1	0
Force x1	1	0	1	1
Measure Temp	1	1	0	0
Measure Temp Dummy	1	1	0	1
Measure Leak	1	1	1	0
Measure V_{REF}	1	1	1	1

2.6.2. FPU DIGITAL OUTPUTS

The outputs are delayed by three clock periods, as explained in Section 2.7.

Mode	*FPO2*	*FPO1*	*FPO0*
Auto x33	0	0	0
Auto x9	0	0	1
Auto x5	0	1	0
Auto x1	0	1	1
Force x33	0	0	0
Force x9	0	0	1
Force x5	0	1	0
Force x1	0	1	1
Measure Temp	1	0	0
Measure Temp Dummy	1	0	1
Measure Leak	1	1	0
Measure V_{REF}	1	1	1

2.7. TIMING



The FPU timing is shown above. The FPU clock is a copy of the LHC 40 MHz clock, generated by the CTRL chip. As the clock is differential, the ideal clock in the figure above represents its "sign". When the *ideal clock* is high, the FPU tracks the signal, and when the *ideal clock* is low, the FPU holds all signals, and selects the multiplexer output. The ADC clock has the same phase as the FPU clock but the signal is sampled by the ADC just as the FPU returns to *hold* from *sample*. There is an 0.5 clock latency between the time when the signal is sampled by the FPU and when digitization commences. The ADC has a two clock plus 9 ns latency, to which the additional 0.5 clock latency of the FPU must be added. This results in an approximately 3 clock latency between when the signal was sampled, and the ADC data are valid. As the FPU output bits (FPO0 ... FPO2) must match the ADC, three clock cycles internally delay the FPU output bits.

2.8. ESD PROTECTIONS

Too prevent electrostatic discharges, the core cell is surrounded by protected bonds pads. Preamplifier and APD leakage current inputs are very sensitive to noise and protected diode leakage current, a special ESD protection scheme was used. At least, on chip transient clamps prevent ESD damages on analog and digital supply lines.

3. FPPA SPECIFICATIONS

3.2. DESIGN CONSTRAINTS

Barrel Readout FPPA

Physics/Experminetal Parameter	***Symbol***	***Value***	***Unit***
Fullscale Energy[1]	E_{MAX}	1.5	TeV
(Target) Light Yield	LY	5	p.e./MeV
APD Operating Gain	M	50	
Spread in Photoelectron Yield	ΔLY	±10% RMS	p.e./MeV
Maximum Noise Level	E_N	40	MeV
APD Capacitance[2]	C_{APD}	<80	pF
Interconnect Capacitance	C_{KAPTON}	<30	pF
Detector Capacitance (2 APD + Interconnect)	C_{TOT}	<190	pF
FPPA Electrical Requirement	***Symbol***	***Value***	***Unit***
(*Derived*) Fullscale Charge	Q_{MAX}	60	pC
(*Derived*) Noise Equivalent Charge	ENC	10000	e^-
(*Derived*) Dynamic Range	DR	>90	dB
Fullscale Voltage (Preamp Output)	V_{MAX}	2	V
(*Derived*) Noise Voltage	V_N	50	μV

[1]Readout in E not E_T [2]Spread in C_{APD} ~ 10%

Endcap Readout FPPA

Physics/Experminetal Parameter	***Symbol***	***Value***	***Unit***
Fullscale Energy[1]	E_{MAX}	3	TeV
(Target) electron Yield[3]	LY	34	e^-/MeV
Spread in Photoelectron Yield[4]	ΔLY	±20% RMS	p.e./MeV
Maximum Noise Level	E_N	100	MeV
Detector Capacitance (VPT + Interconnect)	C_{TOT}	<40	pF
FPPA Electrical Requirement	***Symbol***	***Value***	***Unit***
(*Derived*) Fullscale Charge	Q_{MAX}	16.5	pC
(*Derived*) Noise Equivalent Charge	ENC	3500	e^-
(*Derived*) Dynamic Range	DR	>90	dB
Fullscale Voltage (Preamp Output)	V_{MAX}	2	V
(*Derived*) Noise Voltage	V_N	68	μV

[1]Readout in E not E_T [3]Hamamatsu VPT, 5.5 pC/TeV [4]±10% LY, ±15% VPT

3.3. ELECTRICAL SPECIFICATIONS

FPPA Power Supply

Parameter	*Symbol*	*Value*	*Unit*
Positive Digital FPU Power	Vccd	+5 typ.	V
Positive Digital Output FPU Power	Vcco	+5 typ.	V
Positive Analog FPU Power	Vcca	+5 typ.	V
Positive Preamplifier Analog Power	Vccpa	+5 typ.	V
Negative Analog FPU Power	Veea	-2 typ.	V
Negative Preamplifier Power	Veepa	-2 typ.	V
Negative Digital FPU Power	Veed	0	V
Negative Digital Output FPU Power	Veeo	0	V
Power Dissipation	P	750	mW

Preamplifier

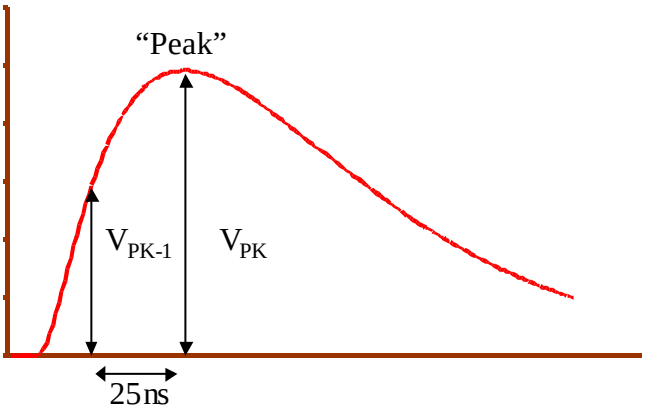
Parameter	*Symbol*	*Value*	*Unit*
Gain Range "5"/Range "1"	G_5	5	
Gain Range "9"/Range "1"	G_9	9	
Gain Range "33"/Range "1"	G_{33}	33	
Gain Tolerance	$\Delta G/G$	±10	%
Preamplifier Pedestal Voltage[5]	V_{PED}	0.7 (min)	V
Pedestal Shift with irradiation	$d_{VPED}/dRad$	50 mV (max)	10 years
Bandwidth Matching for Gain Stages	$\Delta BW/BW$	0.1	%
Pulse shape Matching for Gain Stages[6]	$\Delta r/r$	1	%
Clamp Voltage	V_{CLAMP}^{PA}	2.7	V
Clamp Flatness[7]	$\Delta V_{CLAMPED}$	200	mV

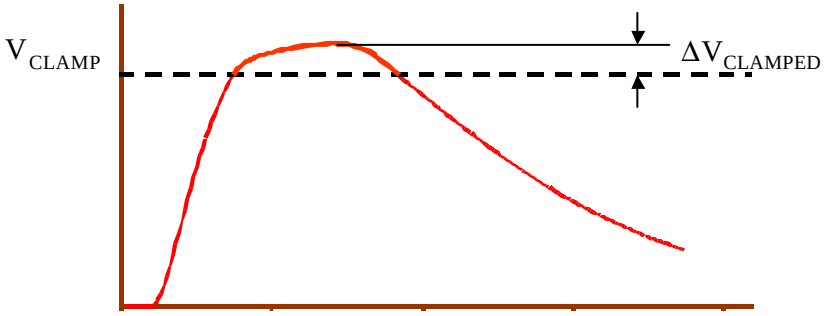
[5]Measured at the output of the preamplifier on the x33 range. The FPU output voltage is then $\left(V_{PED}+V_{33}+V_{OS}^{FPU}\right)/2$

[6]The flatness of the value of r defines the pulse shape matching – r is the ratio of the preamp+gain stage output 25 ns before the peak sample value of the peaking time to that of the peak sample value of the peaking time -.

$$r=\frac{V_{Pk-1}(\text{Peaking time } -25\text{ns})}{V_{Pk}(\text{Peaking time})}.$$

The peak sample must satisfies $V_{PK} > V_{PK-1}$ and $V_{PK} > V_{PK+1}$.



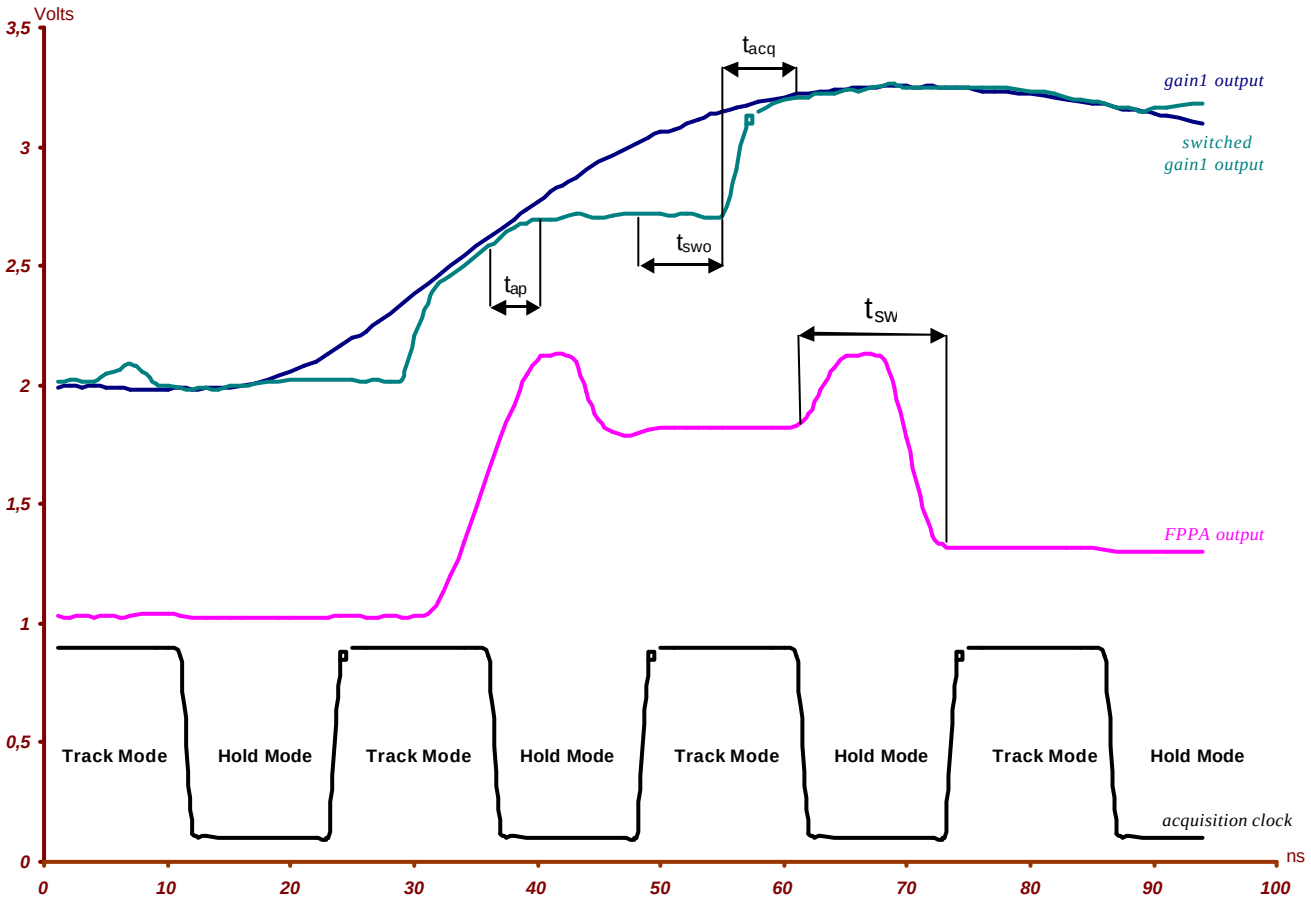


[7]Clamp flatness is the overshoot of the clamped output

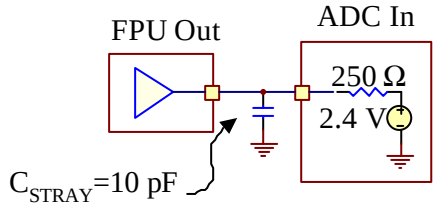
FPU

Parameter	*Symbol*	*Value*	*Unit*
FPU Sampling Frequency	f	40	MHz
FPU Acquisition Time[8]	t_{acq}	6	ns
FPU Switching Time Between range[8]	t_{sw}	12	ns
FPU Aperture Delay Time[8]	t_{ap}	2	ns
FPU Switch-On Delay Time[8]	t_{swo}	7	ns
FPU Droop Rate	V_{DROOP}	0.2	mV /ns
FPU Internal Linearity (deviation from best fit)	Lin(S/H)	0.1	% FS max
FPU Voltage Offset	V_{OS}^{FPU}	10	mV
Comparator Output Rise/Fall Time	$t_{cmp(tr/tf)}$	3	ns
Comparator Overdrive to Switch	V_{OD}		mV
FPU Output Buffer Linearity[9]	Lin(BUF)	0.1	% FS max
FPU Output Buffer Noise	V_N^{FPU}	100	µV
FPU Switching threshold (internally generated)	V_{THRESH}	2.1	V
FPU Total Linearity (Signal)	Lin(FPU)	0.1	% FS max
FPU Output Range	V_{OUT}^{BUF}	1.9 to 2.9	V
FPU S/H clamp (internally generated)	C_{LO}	2.0	V
FPU S/H clamp (internally generated)	C_{HI}	0.5	V

[8] Where t_{acq}, t_{swo},t_{ap} measure S/H only, and t_{sw} measure S/H and multiplexer.



[9] With the FPU Output terminated as shown



Tempeature / Leakage Current Measurements

Parameter	*Symbol*	*Value*	*Unit*
T-Stage TransResistance	R_F[1]	260[9]	kΩ
T-stage Offset (RTI)	I_{OS}[1]	50	nA max
T-Stage Linearity	Lin(T)	0.3	% max
T-Stage Input Voltage	V_{IN}[1]	1.2	V
I-stage Current gain	G(I)	10	$\mu\Omega^{-1}$
I-stage Offset (RTI)	I_{OS}[1]	20	nA max
I-Stage Linearity	Lin(I)	1	% max
I-Stage Input Voltage	V_{IN}[1]	0	V
I-Stage TransResistance	R_F[1]	100	kΩ
Input voltage current sensitivity	dV_{IN}/dI_{IN}	15	Ω

[9] Adapted to value of thermistor (R_{25} = 100kΩ ; β = 3960 K)

Auxilliary Functions

Parameter	*Symbol*	*Value*	*Unit*
ADC Clock Output Central Voltage	V_{CKA}	1.6	V
ADC Clock Output Swing (single output)	ΔV_{CKA}	±400	mV
ADC Clock Output Rise Time	$CKAt_R$	2.5	ns
ADC Clock Output Fall Time	$CKAt_F$	1	ns
ADC Clock Output Delay Time	$CKAt_d$	1.8[10]	ns
ADC Clock Output Duty Cycle	CKA_{cycle}	53[10]	%
ADC Clock Output jitter	CKA_{jitter}		ps
V_{REF} Input Current	$I(V_{REF})$	2	uA
FPU Output Offset Voltage	$V_{3.3}$	3.3	V
FPU Mode Output Delay	t_{DO}^{FPPA}	-1.2[11]	ns

[10] Measured from the ADC clock logic threshold

[11] FPU bits mode are 3 clock latency. Mode Signals are delayed $3\left(\frac{1}{f}\right)+t_{DO}^{FPPA}$

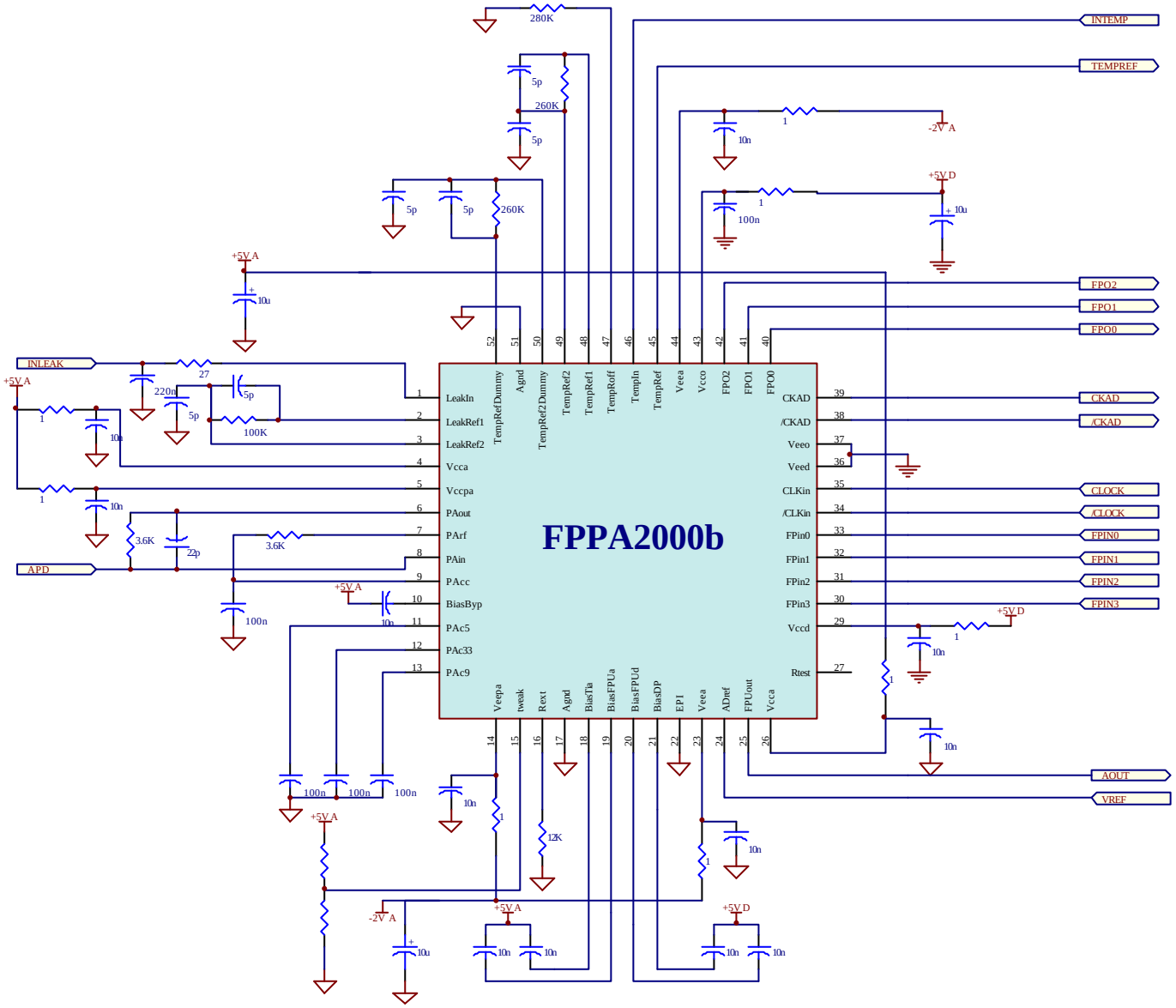
Typical Operating Conditions (LHC)

Parameter	*Symbol*	*Value*	*Unit*
Digital Logic +5V Supply	DVCC	+5.0	V
Analog +5V Supply	AVCC	+5.0	V
Analog –2 Supply	AVEE	-2.0	V
Ambient Temperature (Environment)	T_A	18	°C
Clock Frequency	LHC BCO	40.08	MHz
Minimum anticipated TD (η=0, 10 years)	TD_{MIN}	0.1	MRad
Maximum anticipated TD ($\eta=\eta_{MAX}$, 10 years)	TD_{MAX}	2.5	MRad
Minimum anticipated 1 MeV equivalent neutron fluence (η=0, 10 years)	ND_{MIN}	10^{13}	n/cm^2
Maximum anticipated 1 MeV equivalent neutron fluence ($\eta=\eta_{MAX}$, 10 years)	ND_{MAX}	$5x10^{13}$	n/cm^2

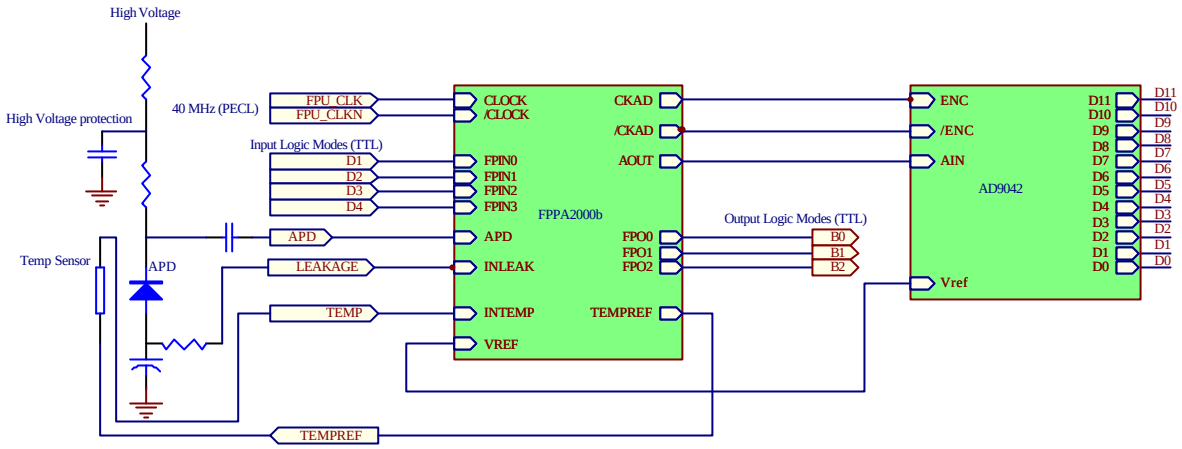
4. FPPA2000 IN USE

4.2. CONNECTING THE FPPA2000-barrel

The FPPA2000b (b for barrel) circuit needs a set of components shown above:



All power supplies must have polarized decoupling capacitors and all inputs power supply must have specific decoupling scheme (capacitor + resistor). Because, power supplies are protected, all FPPA2000b input power supply must be powered in the same time (Analog and Digital).



The FPPA2000b clock inputs are differential PECL level and must be free from jitter. The FPPA2000b clocks output must be connecting directly to the ADC.

To avoid high current from a dead APD, a high voltage filter is used. The APD input pin is isolated from high voltage by a high voltage capacitor.

The APD reference is now fixed by input leakage current stage to ground. This stage has a few ohms impedance. To avoid voltage fluctuations across the APD during light signal, the anode has need grounded capacitor and the leakage input stage need a resistor.

4.3. CONNECTING THE FPPA2000-endcap

Coming soon

4.4. TEST SCHEMATIC

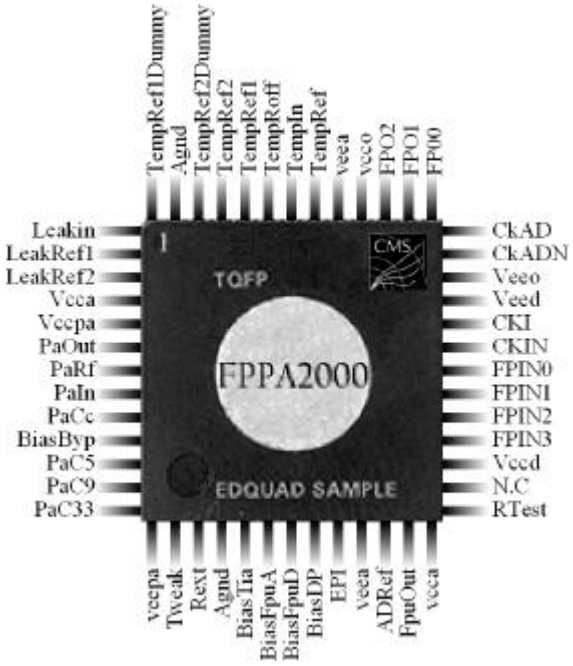
For test, certain limits will only be known after a **pre-production** run has been tested.

5. FPPA PINOUT, PACKAGE AND MECHANICAL INFORMATION

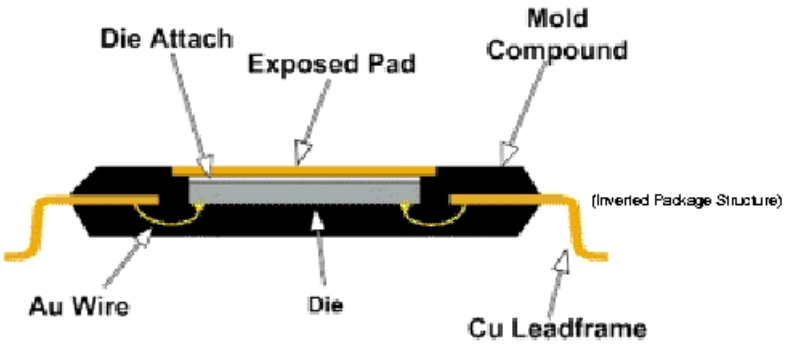
5.2. FPPA PIN FUNCTION DESCRIPTIONS

Pin Name (Mnemonic)	Pin No.	Function
LEAK In	1	Connect to APD anode (not used for VPT)
LEAK R_{F1}	2	Connect to LTIA feedback
LEAK R_{F2}	3	Connect to LTIA feedback
PA Out	6	Connect to preamplifier feedback R_F, C_F
PA RF	7	Used in fixing amplifier operating point
PA In	8	Input - connect to APD cathode/VPT anode through isolating capacitor
PA CC	9	Used in fixing amplifier operating point
BIAS BYP	10	Preamplifier bias generator decoupling capacitor
PA C5	11	DC gain block for x5 decoupling capacitor
PA C9	12	DC gain block for x9 decoupling capacitor
PA C33	13	DC gain block for x33 decoupling capacitor
TWEAK	15	Used in fixing output buffer operating point
R EXT	16	Used in fixing bias generator operating point (I = 2.4V/R)
BIAS TIA	18	Bias generator decoupling capacitor
BIAS FPUA	19	Bias generator decoupling capacitor
BIAS FPUD	20	Bias generator decoupling capacitor
BIAS DP	21	Bias generator decoupling capacitor
AD REF	24	Connect to AD9042 V_{REF}
FPU Out	25	Connect to AD9042 AIN
R TEST	27	Test Resistor. Not used
FP IN3	30	FPU Control Bit 4 (TTL)
FP IN2	31	FPU Control Bit 3 (TTL)
FP IN1	32	FPU Control Bit 2 (TTL)
FP IN0	33	FPU Control Bit 1 (TTL)
CK IN	34	Clock Input (Inverted) (PECL)
CK I	35	Clock Input (Non-inverted) (PECL)
CK ADN	38	Connect to AD9042 /ENCODE (Inverted)
CK AD	39	Connect to AD9042 ENCODE (Non-inverted)
FP O0	40	FPU Digital Output Bit 1 (TTL)
FP O1	41	FPU Digital Output Bit 2 (TTL)
FP O2	42	FPU Digital Output Bit 3 (TTL)
TEMP REF	45	Connect to thermistor
TEMP In	46	Connect to thermistor
TEMP ROFF	47	Used in fixing TTIA offset
TEMP R_{F1}	48	Connect to TTIA feedback
TEMP R_{F2}	49	Connect to TTIA feedback
TEMP R_{F1} Dummy	52	Connect to Dummy TTIA feedback
TEMP R_{F2} Dummy	50	Connect to Dummy TTIA feedback
EPI	22	Clean ground - die topside
VCC A	4, 26	+5V Analog Power Supply (Analog Part)
VCC PA	5	+5V Analog Power Supply (Preamplifier Part)
VCC D	29	+5V Digital Power Supply (Logic Part)
VCC O	43	+5V Digital Power Supply (Logic Output Part)
VEE D	36	0V Digital Power Supply (Logic Part)
AGND	17, 51	Analog Ground
VEE A	23, 44	-2V Analog Power Supply (Analog Part)
VEE PA	14	-2V Analog Power Supply (Preamplifier Part)
VEE O	37	0V Digital Power Supply (Logic Output Part)

5.3. FPPA PINOUT



5.4. FPPA PACKAGE

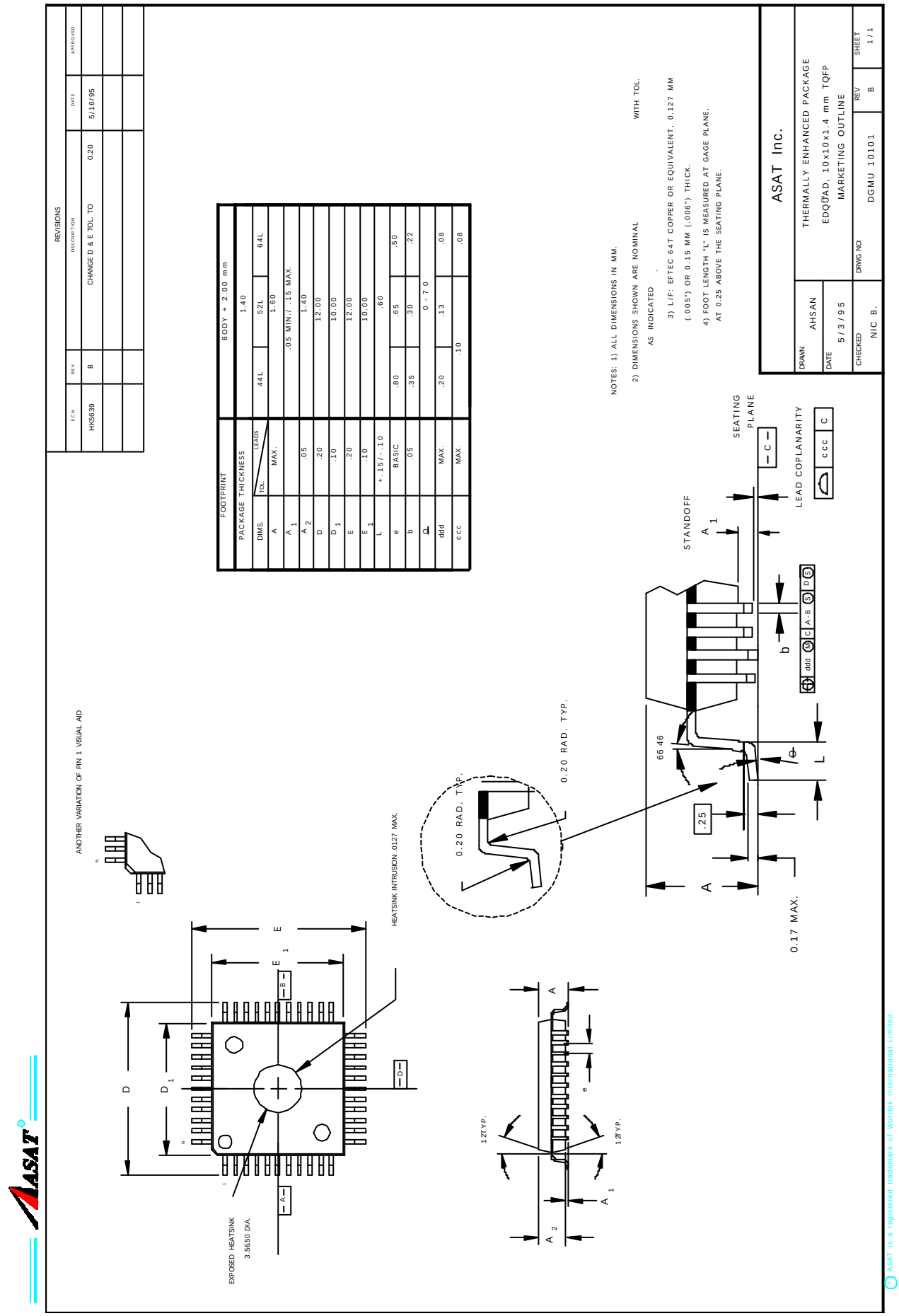


The FPPA will be packaged in a thermally-enhanced, 52-pin 10 x 10 mm^2 Thin Quad Flat Pack.

As shown on the left, the die is mounted upside-down, and is in contact with a metal plate. This allows a better thermal contact in the VFE readout modules. In order to simplify the module covers, the FPPA package has the same height as the ADC package.

5.5. PACKAGE MECHANICAL INFORMATION

Package Type	TQFP ASAT EDQUAD
Package Designation	JEDEC MS-026C BCC-H? ???
Die size x	5600 µ
Die size y	5200 µ
Die thickness	??? µ
Number of bonded pads	52
External lead pitch	0,65 mm
Passivation	Si_3N_4
Die attach	Conductive Epoxy
Bond wire	???



6. REFERENCES

- AD9042 :12 bit, 41 MSPS monolithic A/D converter, Analog Devices Inc.
- Custom Integrated Front-End Circuit for the CMS Electromagnetic Calorimeter, IEEE TNS (coming soon).
- Light-to-Light Readout System of the CMS Electromagnetic Calorimeter, IEEE TNS (coming soon).