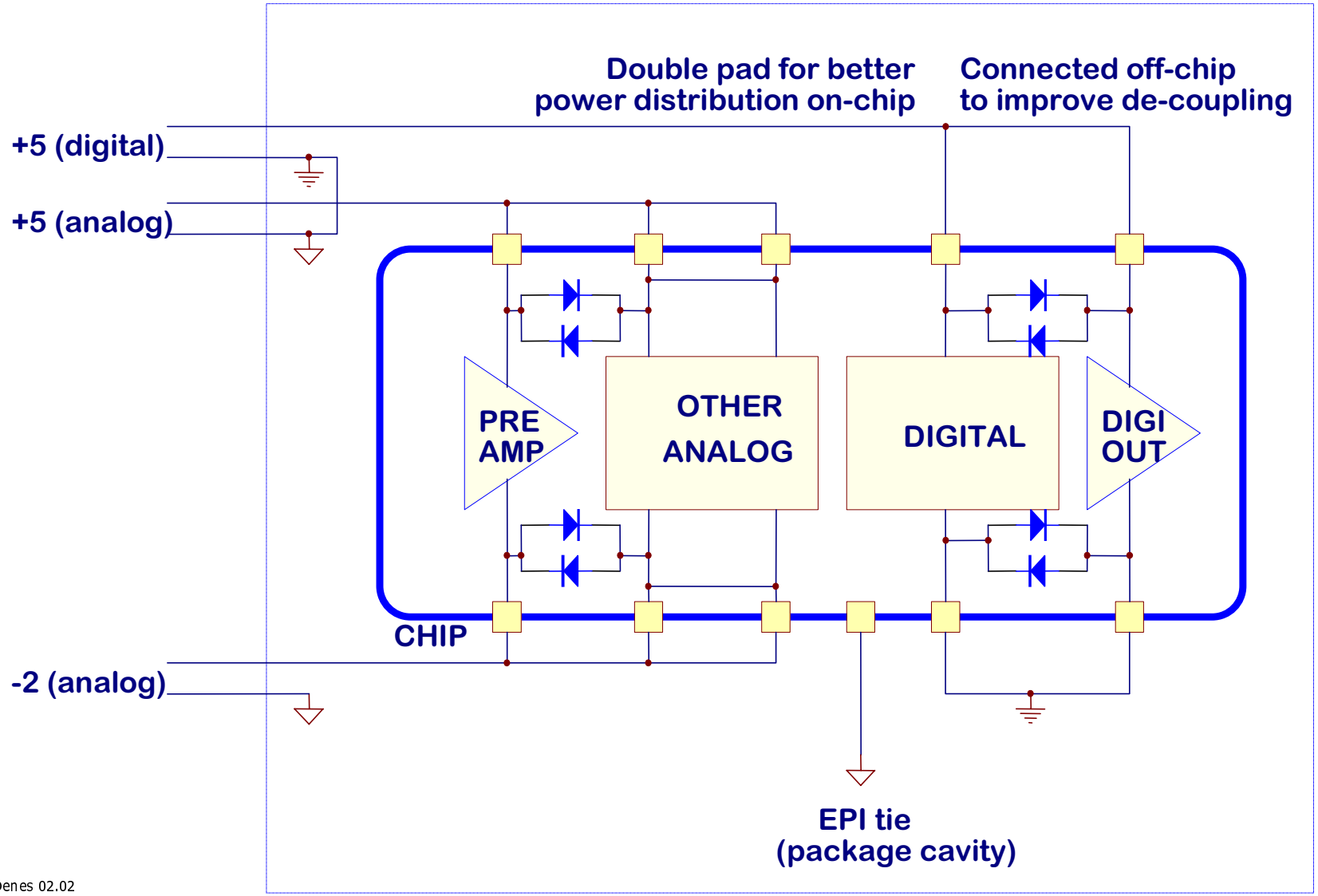
ESD

FPPA2000 ESD Protection developed along Intersil guidelines
Goal is 1500V HBM, satisfying **zap** between *any* two pads

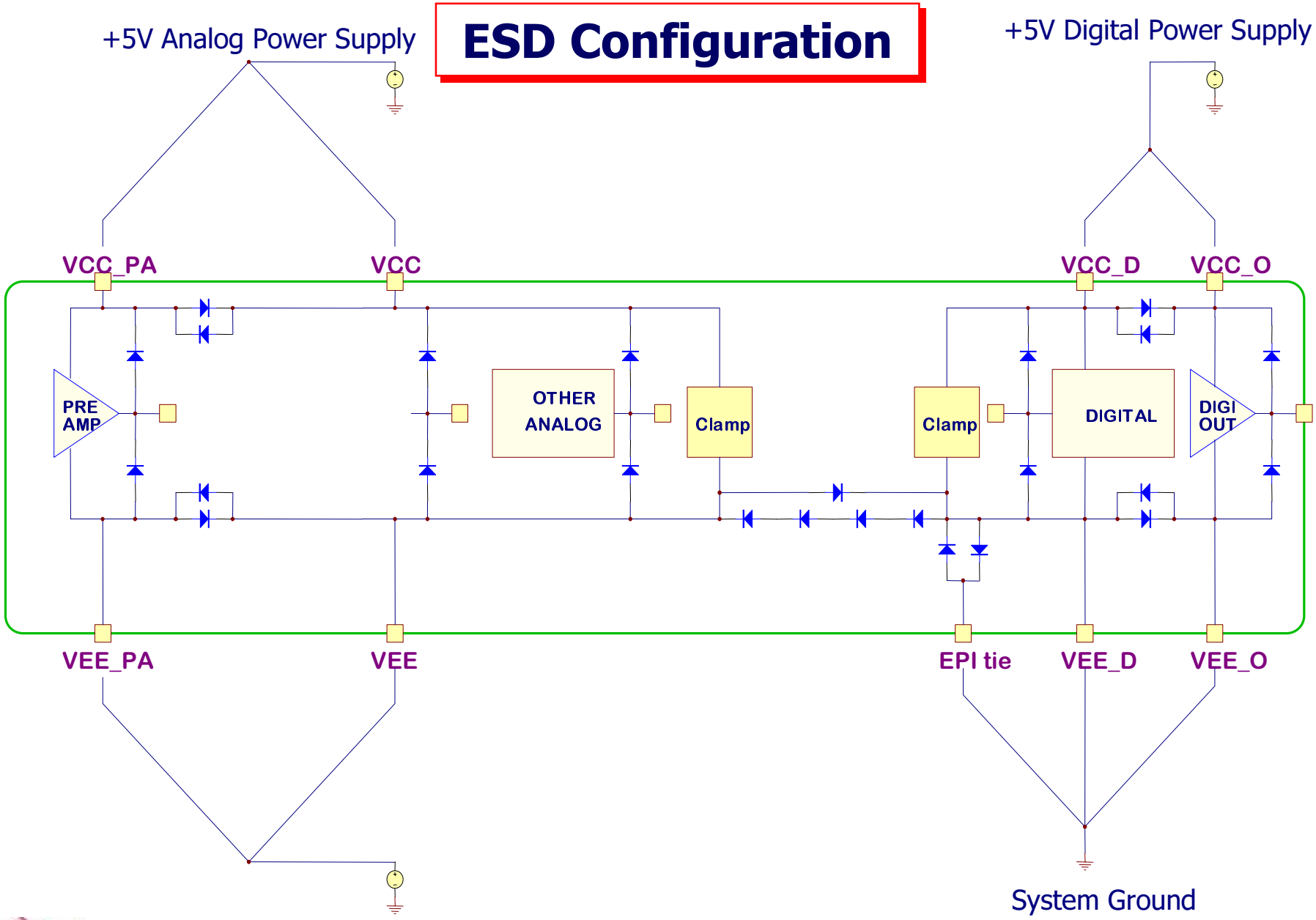
Design kit incorporates special protection diodes
Transient clamps have been added

Analog inputs have additional protection in order to avoid breakdown or excessive current

Power Connections - Chip and Circuit Card



ESD Configuration

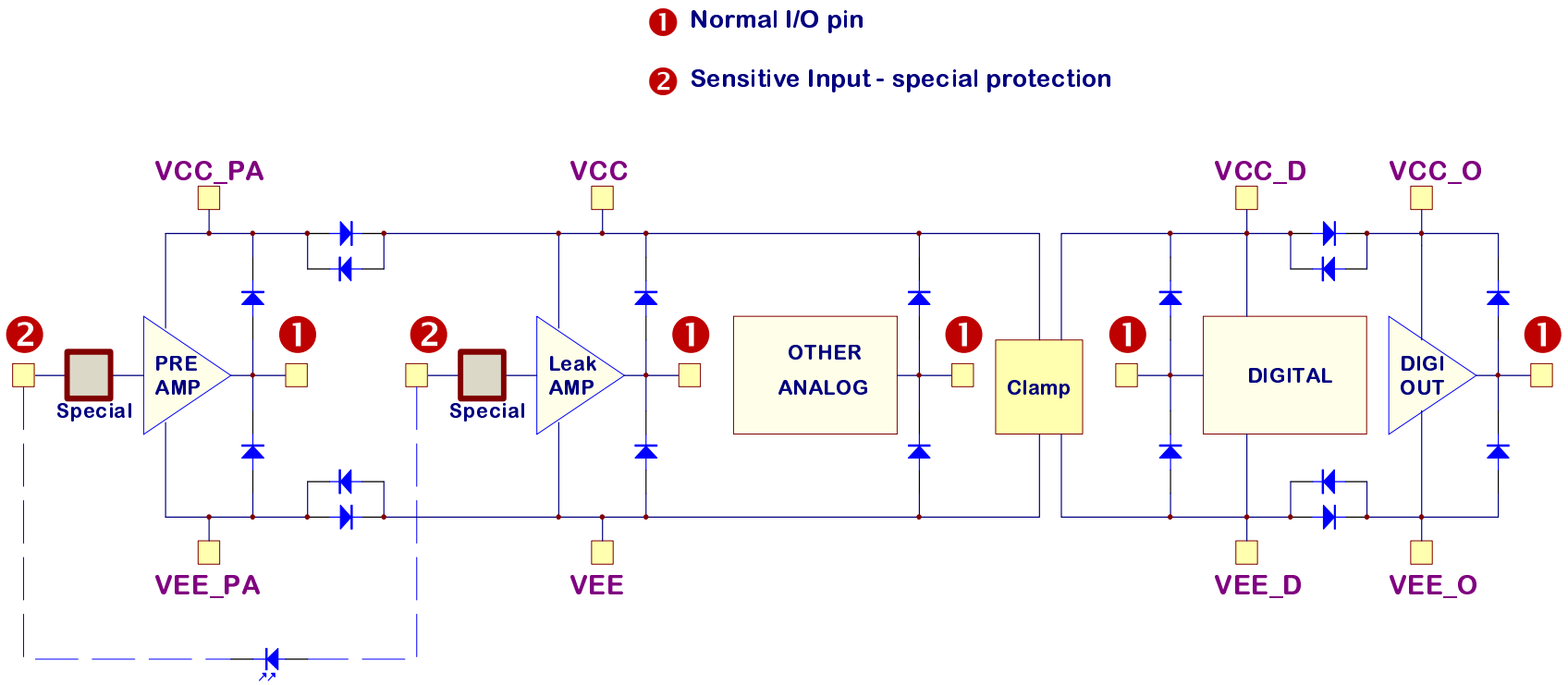


ESD Detail (I.)

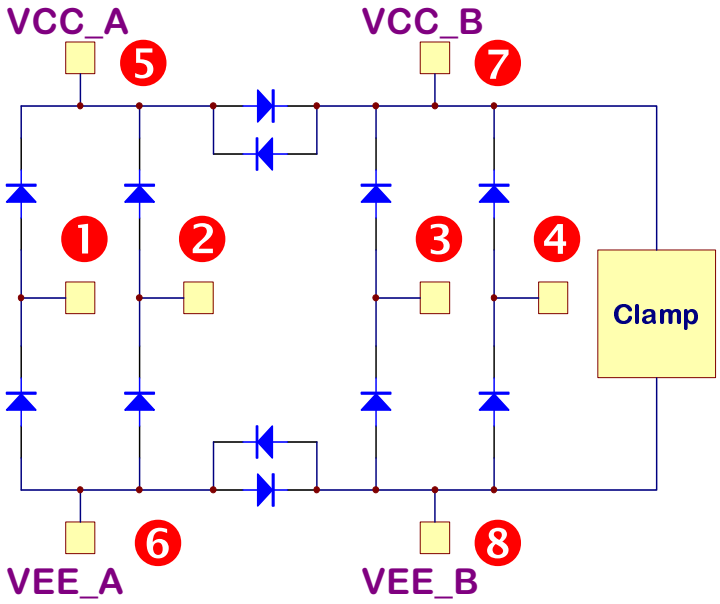
All pins have ESD diodes to V+ and V– ***except*** for the two sensitive inputs

VCC_PA is ESD diode clamped to VCC
VEE_PA is ESD diode clamped to VEE

VCC_O is ESD diode clamped to VCC_D
VEE_O is ESD diode clamped to VEE_O



ESD Detail (II.) Voltage Limits



	Zap ❶↔❷	Zap ❶↔❸	Zap ❶↔❽
❶	❺+V_D	❺+V_D	❺+V_D
❷	❻-V_D	0	0
❸	0	❽-V_D	0
❹	0	0	0
❺	❼+V_D	❼+V_D	❼+V_D
❻	❽-V_D	❽+V_D	❽+V_D
❼	❽+V_C	❽+V_C	❽+V_C
❽	-V_C/2	-(V_C+V_D)/2	-(V_C+2V_D)/2

Voltages at nodes during **ZAP!**

Seems ok.

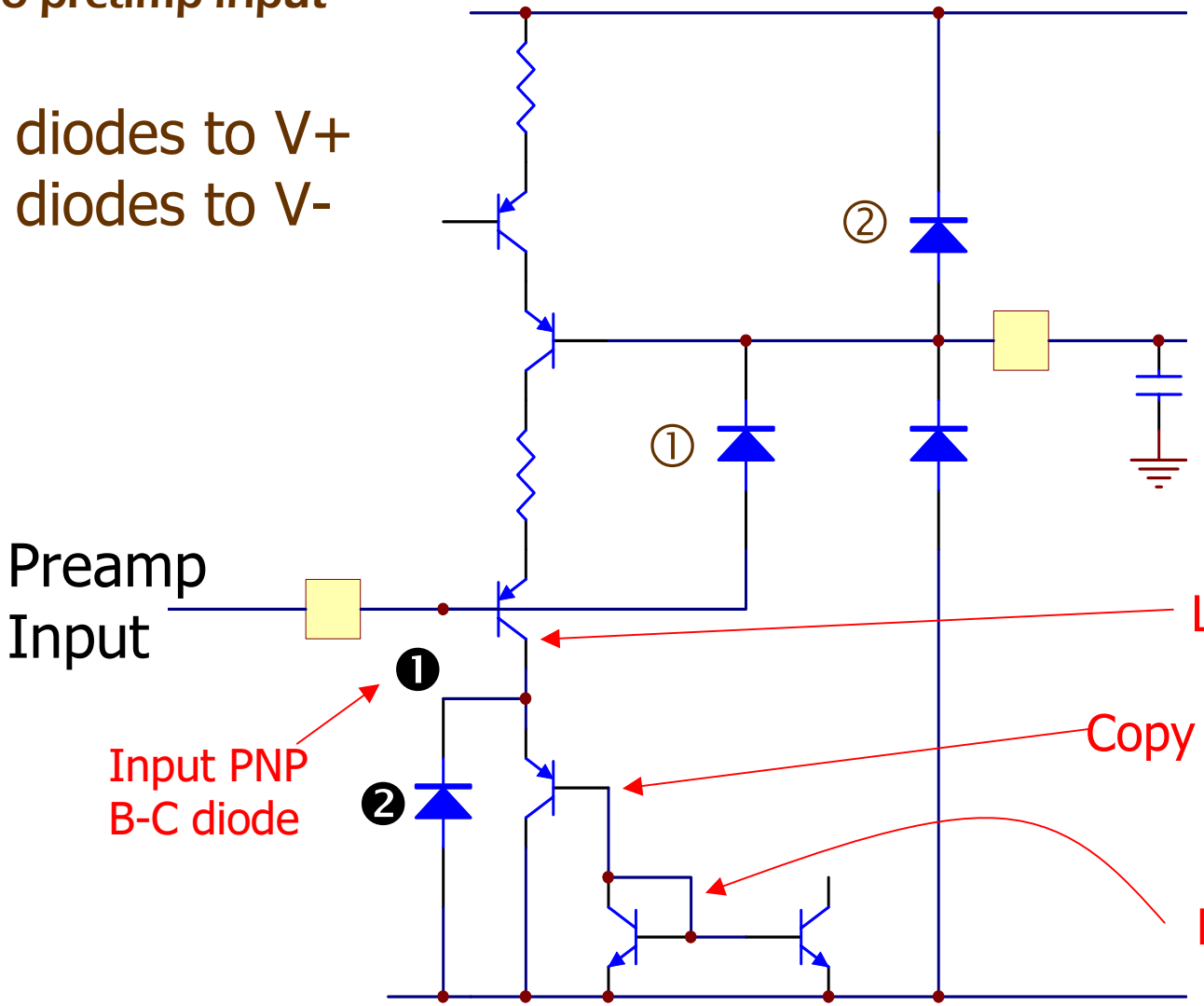
V_D is one diode drop
V_C is the voltage across the supply clamp

Preamp Input - ESD

Goal: avoid coupling noise (esp. V_{CC}/V_{EE}) into preamp input

② diodes to V+

❷ diodes to V-



Sets baseline

take advantage of external C to reduce coupling via diode

Large input PNP

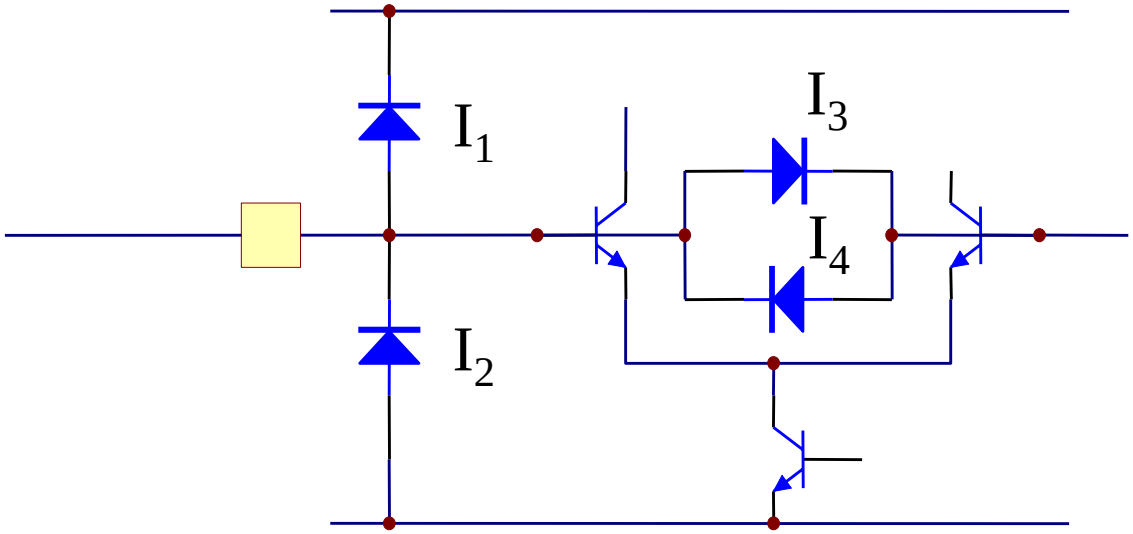
Copy of large input PNP

Input PNP B-C diode

Base current comp.

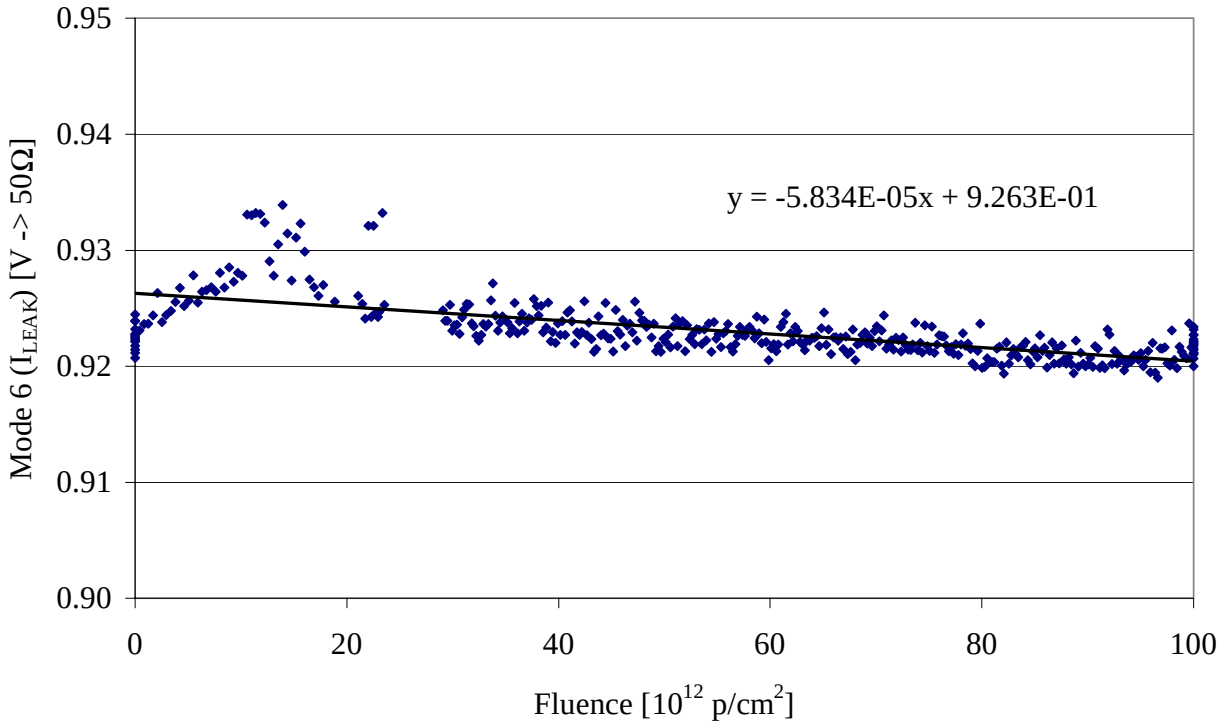
Sensitive Differential Pair Input

Photodetector leakage current measurement
Want error ≤ 20 nA.
Concern is radiation-induced leakage current in ESD diodes
(but tests indicate that this actually works fine →)



Irradiation Results

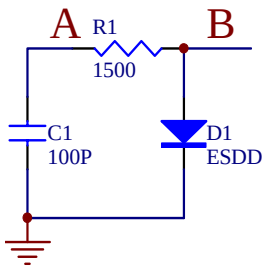
FPPA2000 irradiation at LBL 88” cyclotron
Sensitivity of circuit ~ 0.5 nA/LHC_year (i.e. no problem)

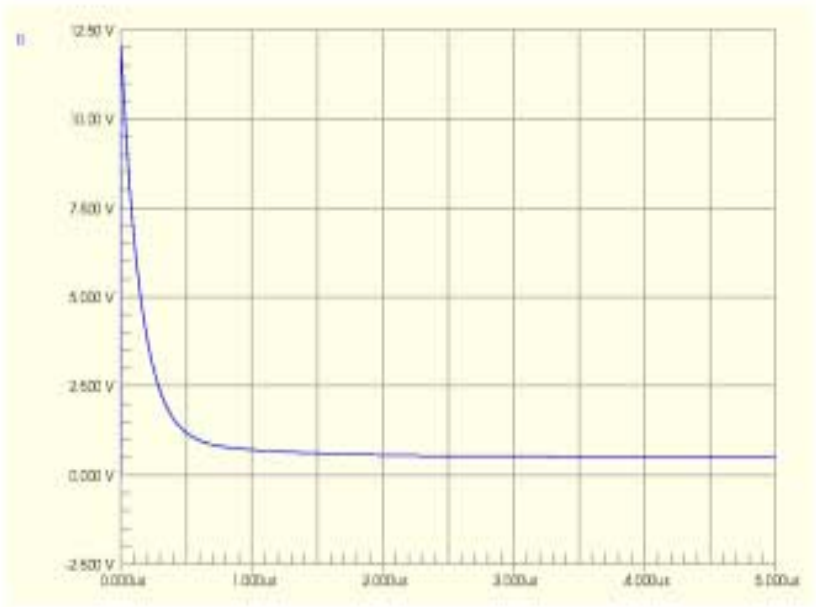


ESD Diode Rules

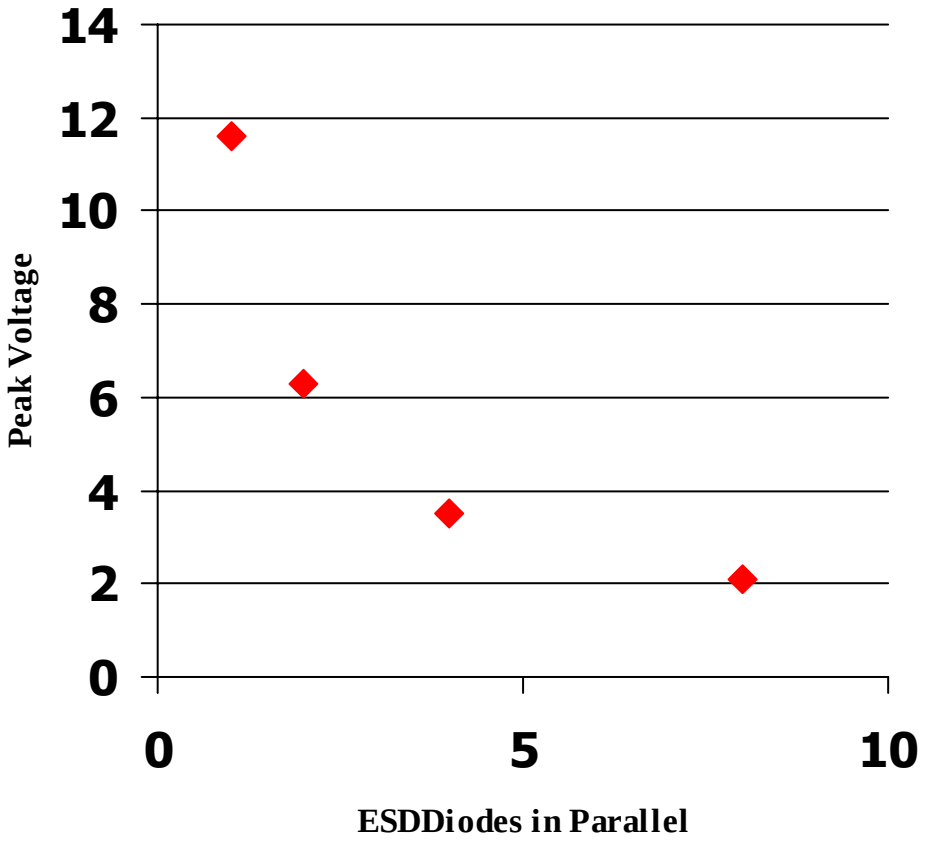
2kV HBM

100 pF
IC = 2kV

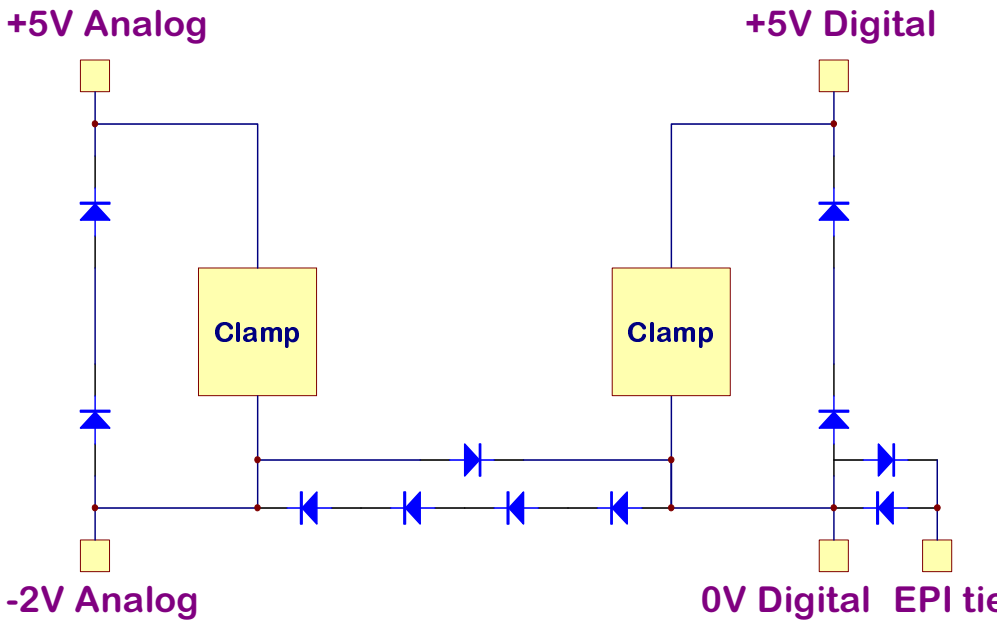


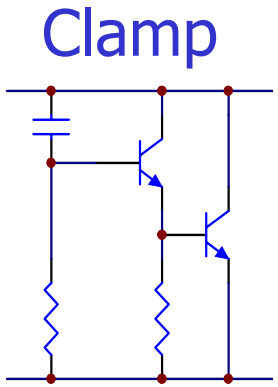


V_{PEAK} = 12Volts/N
for N diodes in parallel
To limit to 3V, use at least 4 diodes



Supply Clamps





Transient clamps from V_{CC} to V_{EE} (analog and digital)
No diode clamp between analog and digital V_{CC} (Power supply startup)
(zaps between V_{CC} pins clamped via V_{EE} diodes and one transient clamp)
Analog V_{EE} (-2V) diode clamped to Digital V_{EE} (0V)
EPI tie pad diode clamped to (digital) 0V