EE Workshop, 12 - 14 March, 2002 http://hepwww.rl.ac.uk/CMSecal/Workshops.htm

GOALS

- Agree and define the scope of the next EE EDR
- Agree the date for the next EE EDR
- Agree/update the design parameters for EE
- Present and record the current mechanical design for backplates, env screen, ring flange, EE/HE mounting, installation in CMS.
- Present and record the current services requirements.
- Record the issues that need resolving before the next EE EDR
- Assign an action list of tasks that need to be completed before the EDR, and by whom.

Scope of the next EE EDR

Approve the design of :

> the Dee Backplates

➤ the Positional Spacers

> the Environmental Screen

> the Ring Flange

and give approval to proceed to tender.

Present the tooling/installation scenario in CMS and show full compatibility.

Pre EE EDR meeting, compatibility with CMS, Fri 17 May, 2002 EE EDR, 3-4 Sep, 2002

EE Design Requirements

1) Installation/Dismounting

It must be possible to mount/dismount a single Dee to HE with or without the beam pipe in position.

It must be possible to mount/dismount a single Dee with or without the second Dee in its final position.

2) Maintenance of the Dees

Following from 1) if one Dee has a problem it must be possible to mount/dismount the Dee without moving or uncabling the neighbouring Dee.

The guidelines imply that a Dee would first be loosened (slightly) and then moved horizontally away from the other Dee, along the x axis.

The Dee would then be brought forward (towards the IP) to clear the HE nose before being taken away by crane.

EE Workshop, 12 - 14 March, 2002

Actions :

- Agree/update the design parameters for EE None changed during workshop Use of 10 mm shim by EE possible, case must be made
- Holes for EE to HE mounting, needed by Nov, 2002
 Avoid drilling after HE megatyles installed
 Need EE/HE template or equivalent
 Need final array of holes specified
 JH/AS
 Holes for cable trunking on HE, also Nov 2002 ?
 AS
- Dee/positional spacers strongly advise done by same company A tender option – company to do pre-assembly Choice of alloy very important for backplate stability

Actions (contd)

- Need agreement for h = 3.
 h = 3 area agreed during workshop
- Not a good idea to design EE without the service constraints Don't separate EE patch panel design from the 53° crack issues Manifolding difficulty at HE nose – need many pipes, cables.
- Mounting of Dee not yet defined.
 Workshop made progress. HE holes agreed.
 Want table of hole/size coordinates signed off
 JH/AS
 Deformation of support riser when demounting Dee worry
 AS
- Need to include radiation shielding on dismounted Dee AS
- Temperature stabilization of SE during Dee maintenance

http://hepwww.rl.ac.uk/CMSecal/Workshops.htm Workshops

EE Workshop, 12-14 March, 2002

Conclusions and action list	D Cockerill, <u>pdf</u>
Services issues	J Greenhalgh, ppt
Agenda	doc
Tue, March 12, 2002	
Goals	D Cockerill, <u>doc</u>
Pre EDR intro, EE planning & critical paths	J Greenhalgh, ppt pdf
Proposed scope of next EDR	D Cockerill, <u>doc</u>
Design criteria for EE mounting/dismounting	D Cockerill, <u>doc</u>
Wed (am), March 13, 2002	
EE Mechanical design	J Hill, doc
Environmental Screen	A Levine, <u>dxf-zip</u>
Dee Assembly	G Barber, doc
EE fibre optic routing, Dee MEM box	M Anfreville, doc
Mechanical FEA - background	J Greenhalgh, A Abramov <u>ppt pdf</u>
EE/HE FEA analysis	A Abramov, doc

Installation in CMS	A Surkov, doc
Wed (pm), March 13, 2002	
ECAL cooling system	P Baillon, <u>ppt</u>
EE Thermal issues	J Greenhalgh, ppt pdf
Thermal FEA, backplate	A Riabov, J Greenhalgh ppt
Thermal FEA, front environmental screen	A Riabov,J Greenhalgh, ppt
Thermal FEA, outer environmental screen	A Riabov,J Greenhalgh, ppt
Thermal FEA, eta = 3 region	I Wichrowska-Polok, ppt
Thermal FEA, eta = 3 region, cross section	I Wichrowska-Polok, <u>doc</u>
EE Services	S Bally, <u>pdf</u>
EE Services	P Ingenito, <u>pdf</u>
EE Services	J Greenhalgh, ppt pdf
Thursday, March 13, 2002	
Overview - ECAL Electronics	P Sharp, doc
Electronics integration in EE	A Lodge, doc
Low voltage issues	W Lustermann, doc
VPT High voltage system	R Brown, ppt
VPT mass production status	R Brown, ppt
EE Trigger Issues	K Bell, doc

Dee mechanics Mechanical FEA – encouraging 2 tonne maximum load on any bolt Safe to go ahead with current design for EE to HE mounting

Actions:

JH/AL/AS

- Define slots thru backplate
- Holes on rear of backplate for studding to support moderator/electronics
- Eta=3 holes,
- Side panel holes
- Env. Screen holes

Dee Assembly

• A fully prototyped SC loader to be tested before the EDR GB

Mechanical design issues:

- Any Dee in any position on CMS not clear
- Electrical insulation from HE needs discussion. May CMS Electronics workshop.
- Thermal insulation, HE to EE needs discussion

Clearance of Dee past SE cone	
Clearance of 'bump stop' during mounting/dismounting	AS/JH
Complex dismounting/mounting interactions with SE	AS/PW
Question of side plate, for cooling at test beam	
Radius of edge of environmental screen for SE cables	
Check clearance definition for outer envelope of environmental screen	AS/GF
• Problem of interference with support ring and fixed fittings over HE nose	AS
Question of dummy SE	
Question of Dee 'zip' to join environmental screens of adjacent Dees	

Thermal issues

- **h** = 3 OK. No cooling pipes needed on inner thermal screen
- Environmental screen OK in current design no changes needed

Services

- Route from cooling station to detector described
- Must interact closely with integration group S Bally, P Ingenito
- Pipe insulation more important for EE have thinner pipes than EB OT
- 'Double MEM' box integration problem of connectivity PI/MA

Electronics

- HV system for VPTs layout & requirements **Component irradiation results**
- VPT production status reported

Integration of electrical/optic services

• LV services – need to know which scheme • Fibre optic services – need to know which type • Integration of new electronics • Cooling of all components • Major issue - forming trigger towers in the EE Easter – agree pattern, May/June – simulation results Max allowed temperature of chips

Delay impeding design Delay impeding design Unresolved Unresolved Unresolved

Unresolved