Study of LVDS Serial Links for the ATLAS Level-1 Calorimeter Trigger

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Abstract:

This paper presents an evaluation of the proposed LVDS serial data transmission scheme for the ATLAS level-1 calorimeter trigger. Approximately 7000 high-bandwidth links are required to carry data into the level-1 processors from the preprocessor crates. National Semiconductor's Bus LVDS serialiser/deserialiser chipsets offer low power consumption at low cost and synchronous data transmission with minimal latency. Test systems have been built to measure real-time bit error rates using pseudo-random binary sequences. Results show that acceptable error rates better than 10^{-13} per link can be achieved through compact cable connector assemblies over distances up to 20m.

Summary:

The ATLAS level-1 calorimeter trigger requires approximately 7000 high-bandwidth serial links to transfer data from the preprocessor into the algorithmic processor systems. Each processor module must receive data in excess of 4 Gbyte/s over these links, with minimal latency and a bit error rate (BER) better than 10^{-10} for each link.

It was originally proposed to use HP G-link chipsets, which have performed well in tests, but do lead to a very high power density on the processor modules. This high power dissipation would require serious attention to module and crate cooling. LVDS links offer much lower power consumption, and the National Bus LVDS serialiser/deserialiser chipsets DS92LV1021/DSLV1210 etc. are easily interfaced to the trigger system while transmitting data synchronously with minimal latency.

Three separate test systems were produced. These involved up to eight channels in parallel, and measured BERs over electrical links using various cable types with lengths from 10m to 20m. Test systems were designed to transmit and check pseudo-random and repetitive data patterns in real-time in order to achieve the statistics required for measurements of very low BERs.

Several types of cable and connector were also evaluated for use within the ATLAS environment. The processor modules will share data via a high-speed backplane, and the LVDS links will be

connected through this backplane in order to allow easy installation and replacement of modules. Compact cable assemblies are needed because of the high channel count per module: up to 96 LVDS channels per module are required and each 9U processor module requires up to 830 backplane pins.

The final installation within ATLAS requires inter-crate links over distances of 10m to 15m, and a low BER is crucial for these links in order to minimise false triggers. For minimum latency, only error detection, not correction, is possible. To minimise the error rates, the cable assemblies being considered require some form of equalisation for the attenuation at high frequencies, as the raw data rate on each link is 480 Mbit/s. Both active and passive pre-compensation techniques at the transmitter have been investigated. BERs better than 10^{-13} per link have been achieved with cable lengths from 10m to 20m even with simple and straightforward L-R equalisation.

Experience showed that use of these parts was not straightforward, operating as they are at the limit of their specified data rate. The causes of power supply noise must be kept to the minimum, and board layout is critical. In particular, it is important to ensure that the transmitter clock has a low level of jitter. However the problems encountered have been understood and solutions found.

In conclusion, the LVDS links form a viable scheme for transfer of large volumes of data, having the advantages of low latency, low power and low cost. They also offer high-density connectivity, which is essential for compact cable plant. Prototype processors are now being designed that will incorporate a large number of such links.