The performance of a Pre-Processor Multi-Chip Module for the ATLAS Level-1 Trigger

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Abstract:

We have built and tested a mixed signal Multi-Chip Module (MCM) to be used in the Pre-Processor of the ATLAS Level-1 Calorimeter Trigger. The MCM performs high speed digital signal processing on four analogue trigger input signals. Results are transmitted serially at a serial data rate of 800 MBd. Nine chips of different technologies are mounted on a four layer copper substrate. Analogue-to-digital converters and serialiser chips are the major consumers of electrical power on the MCM, which amounts to 7.5 Watts for all dies. Special cut-out areas are used to dissipate heat directly to the copper substrate. In this paper we report on design criteria, chosen MCM technology for substrate and die mounting, experiences with the MCM operation and measurement results.

Summary:

The ATLAS experiment requires a highly selective trigger system with optimal efficiency. The event selection at ATLAS will be achieved by a three level trigger system. The first level trigger (Level-1) is a fast pipelined system for the selection of rare physics processes. It achieves a rate reduction from the 40 MHz LHC bunch crossing rate down to the Level-1 accept rate of 75 kHz (100 kHz upgrade). This is done by searching for trigger objects within a total Level-1 trigger latency of 2.0 us. The number of presummed analogue calorimeter signals which are used as input to the Level-1 trigger is about 7200.

Regarding the timing constraints and the large number of analogue signals, the Level-1 trigger needs a hard-wired front-end to perform fast signal processing on all analogue input signals in parallel. This system, which is referred to as Pre-Processor system, provides the input data for the Level-1 trigger algorithms and it performs the readout of data on which the Level-1 trigger has based its decision.

The motivation behind the usage of a Multi-Chip Module (MCM) technology inside the Pre-Processor system is the high number of channels, which must be processed by each Pre-Processor board (64 signals), and the high number of semiconductor devices per printed circuit board. Hence, a MCM technology is essential for the Pre-Processor system to realize a compact system architecture. MCMs represent a technique whereby bare dies and their interconnections are combined inside a single package. The MCM contains both analogue and digital devices. In total it comprises nine dies: two dual FADCs, four Front-End ASICs performing the pre-processing, one multipurpose level conversion ASIC (Finco), and two high speed gigabit transmitter dies from Hewlett Packard (Glink) running at 1.6 GBd.

The design process of the MCM multi-layer structure is based on an industrial available production technique for high density printed circuit boards. This process, called TwinFlex, is characterized by its usage of plasma drilled Micro-Vias for interconnection between layers and its combination of small feature sizes and prices.

One of the most challenging tasks in the MCM design is the thermal management. The increasing of the packaging density and the use of high power dies leads to the exponential nature of component failure rates with temperature. Therefore the dies on the MCM need different thermal resistance from the chip to the case. This difference has been achieved by using a thermal cutout for the gigabit serial transmitter and thermal vias for the FADCs. The total power consumption of the MCM is about 7.5 W.

We will present design criteria, chosen MCM technology for substrate and die mounting and experiences with the MCM operation. System measurements will demonstrate the performance of the Pre-Processor relying on this Multi-Chip Module technology.