One Size Fits All: Multiple Uses of Common Modules in the ATLAS Level-1 Calorimeter Trigger

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Abstract

The architecture of the ATLAS Level-1 Calorimeter Trigger has been improved and simplified by using a common module to perform different functions that originally required three separate modules. The key is the use of FPGAs with multiple configurations, and the adoption by different subsystems of a common high-density custom crate backplane that takes care to make data paths equal widths and includes minimal VMEbus. One module design can now be configured to count electron/photon and tau/hadron clusters, or count jets, or form missing and total transverse-energy sums and compare them to thresholds. In addition, operations are carried out at both crate and system levels by the same module design.

Summary

The ATLAS Level-1 Calorimeter Trigger executes trigger algorithms in two parallel subsystems: Cluster Processor (CP) and Jet/Energy-sum Processor (JEP). Cluster Processor Modules identify electron/photon and tau/hadron clusters, sending the numbers found to merger modules that sum cluster multiplicities for 16 thresholds, first by crate and then for the four-crate subsystem. In the original design these were Cluster Merger Modules, fed by cables to a separate crate. Jet/Energy Modules (JEM) identify jets, and also sum transverse energy and its components over small regions. The numbers of jets found are sent to merger modules that sum jet multiplicities for eight thresholds, first by crate and then for the two-crate subsystem. In the original design this was done by Jet Merger Modules in each crate, fed via the backplane. In parallel, transverse-energy sums were formed by Sum Merger

Modules in each crate, also fed via the backplane, followed by subsystem summing and comparison of total and missing transverse energy with sets of thresholds.

The functionality of Cluster and Jet Merger Modules was very similar, so first those two designs were unified. A simulation showed that data signals could be transmitted over the full backplane width at 40 MHz single-ended (mandatory due to pin-counts), so the same in-crate layout could be adopted for both the CP and the JEP. It was then shown that the energy merging could be done by the same Common Merger Module (CMM) since the 36-bit wide JEM transverse-energy information could be compressed to 24 bits without significant effect on trigger performance. The FPGA code for summing multiplicities, or for computing total and missing transverse energy, could also run in the same FPGAs. The final rationalisation was to adopt a common high-density custom backplane for both processors. Although this required careful module design, it has advantages for the trigger in addition to simplifying it.

There are two CMMs for counting hits or adding transverse energy in each crate. Which operations they carry out is determined automatically by crate and slot occupied. To keep to one design, all modules have facilities for carrying out the final subsystem-wide merging, even though only four of the 12 CMMs are needed for this function.

Pins on the common backplane are at a premium (820 pins/module, 5 rows at 2 mm pitch), and full VMEbus cannot be accommodated. Therefore a minimal set of VME lines is used. Inter-module fan-in/fan-out and input data to the CMMs occupy most of the pins, while timing signals and a CANbus for monitoring voltages and temperatures are also present.

This backplane and CMM arrangement has allowed addition of new trigger algorithms, namely: forward jets, approximate total transverse energy in jets, and total transverse energy exceeding local thresholds. The programmability of the logic allows other variations to be added later.

In addition, two other modules perform multiple roles. A common Readout Driver (accompanying paper) handles both readout data and level-1 trigger regions-of-interest in both CP and JEP, and a common Timing Control Module will service the CP, JEP, and also the Preprocessor subsystem.