Prototype Readout Module for the ATLAS Level-1 Calorimeter Trigger Processors

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Abstract

The level-1 calorimeter trigger consists of three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The CP and JEP will receive digitised calorimeter trigger-tower data from the Preprocessor and will provide trigger multiplicity information to the Central Trigger Processor and region-of-interest (RoI) information for the level-2 trigger. It will also provide intermediate results to the data acquisition (DAQ) system for monitoring and diagnostic purposes. This paper will outline a readout system based on FPGA technology, providing a common solution for both DAQ readout and RoI readout for the CP and the JEP.

Summary

The ATLAS level-1 Calorimeter Trigger consists of three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The CP and JEP will receive digitised calorimeter trigger-tower data from the Preprocessor, and will provide trigger multiplicity information to the Central Trigger Processor via Common Merger Modules (CMMs; accompanying paper). Using Readout Driver (ROD) modules, the CP and JEP will also provide region-of-interest (RoI) information for the level-2 trigger, and intermediate results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

The ROD module for both the Cluster Processor and the Jet/Energy-sum Processor is based on FPGA technology. We have designed these modules to be common to both subsystems, using appropriate firmware to handle several different types of data: RoIs, and DAQ data for both the CP and the JEP.

The collection of both DAQ and RoI data starts at the processor FPGAs on the processor modules, where for every LHC bunch-crossing data are captured in dual-port RAMs. They are transferred from these RAMs to FIFOs, following a level-1 accept signal received from the Central Trigger Processor via the Timing Control Module. Dual-port RAMs and FIFOs are implemented on the FPGAs. Data from up to 20 of these FPGAs on a processor module are merged onto a single high-speed serial link (HP G-link).

The prototype ROD module receives data from four processor modules. It processes and stores the data (with zero suppression if required) in FIFO buffers, formats the data to ATLAS DAQ fragments, and transmits them to DAQ and to the level-2 trigger via S-links at the level-1 accept rate. The data that are sent on the S-links can be spied on for monitoring, and are available on dual-port memories to be read out to a single-board computer via VME for analysis. If more processing power is required, a PCI mezzanine card (PMC) processor can be plugged onto the module.

The prototype ROD is implemented as a triple-width 6U VME module with four common mezzanine card (CMC) positions (two either side): one G-link receiver CMC card interfacing to four processor modules, two S-link positions for DAQ and RoIs, and one position for a commercial PMC co-processor card. It also hosts a TTC receiver card with a CERN TTCrx chip to supply the 40 MHz clock, level-1 accept, and other signals such as bunch-crossing number, event number, trigger type, etc.

Firmware for CP readout to DAQ and RoI readout to the level-2 trigger has been developed and tested, and initial integration tests have been carried out with the RoI builder (ROIB) and the readout subsystem (ROS). The experience gained from this prototype module will benefit the design of the final 9U production ROD module.