The ATLAS Level-1 Calorimeter Trigger Architecture

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We present the architecture of the ATLAS Level-1 Calorimeter Trigger system, which has been improved and simplified by adopting common approaches for data distribution, result merging, readout, and slow control across the three different subsystems. The result is that a significant amount of common hardware is utilized, yielding substantial savings in cost, spares, and development effort. A custom, high-density backplane has been developed with data paths suitable for both the em/tau cluster processor and jet/energy-summation processor subsystems. Common modules have also been produced for TTC, CANbus and VME interfaces with the backplane. A common data merger module uses FPGAs with multiple configurations to perform electron/photon and tau/hadron cluster multiplicity summation, sum jet multiplicities, or to produce total and missing transverse energy sums. The same merger module design also performs both crate and system level operations. FPGAs with multiple configurations have also made possible a common readout driver (ROD) used by all of the subsystems to send input, intermediate and resuts data to the data acquisition system as well as region-of-interest (RoI) data to the level-2 trigger. Extensive use of FPGAs throughout the system make the trigger flexible and upgradable, and certain architectural choices have been made to reduce the number of inter-crate links and make the hardware more robust.