ATLAS Level-1 Calorimeter Trigger: Subsystem Tests of a Prototype Cluster Processor Module

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Abstract

The Level-1 Calorimeter Trigger consists of a Preprocessor (PP), a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce trigger multiplicity and Region-of-Interest (RoI) information. The trigger will also provide intermediate results to the data acquisition (DAQ) system for monitoring and diagnostic purposes by using Readout Driver (ROD) Modules. The CP Modules (CPM) are designed to find isolated electron/photon and hadron/tau clusters in overlapping windows of trigger towers. Each pipelined CPM processes 8-bit data from a total of 128 trigger towers at each LHC crossing. Four full-specification prototypes of CPMs have been built and results of complete tests on individual boards will be presented. These modules were then integrated with other modules to build an ATLAS Level-1 Calorimeter Trigger subsystem test bench. Realtime data were exchanged between modules, and time-slice readout data were tagged and transferred to the ROD at a trigger rate up to 100 kHz. Tests results have been successful and the CPM's present design is close to the final production design.

Summary

The ATLAS Level-1 Calorimeter Trigger system consists of three subsystems, namely the Preprocessor (PP), electron/photon and tau/hadron Cluster Processor (CP), and Jet/Energy-sum Processor (JEP). The CP and JEP will receive digitised calorimeter trigger-tower data from the PP, and will provide trigger multiplicity information to the Central Trigger Processor via Common Merger Modules (CMM). Using Readout Driver (ROD) modules, the CP and JEP will also provide Region-of-Interest (RoI) information for the Level-2 Trigger, and send input data, intermediate and final results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

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The CP system has to process 6400 trigger towers. A Cluster Processor Module (CPM) has been designed to fully process 128 of these towers. Input data consist of 400 Mbit/s LVDS signals coming from the Preprocessor Module (PPM). In order to process overlapping 4x4 trigger-tower windows, massive fanout of these data is required, both on each CPM, and to its immediate neighbours. Data are deserialised and converted to a 160 Mbit/s single-ended serial format for use on board, and to be sent to neighbouring CPM via a custom-built backplane. Eighty-four trigger towers, of both e.m. and hadronic data, must be handled to implement electron/photon and tau/hadron cluster-finding algorithms in a single chip that processes eight overlapping trigger-tower windows. FPGA technology has been chosen to implement the code in this so-called CP chip. Each CP chip flags which e.m./tau thresholds, among 16, have been passed by an isolated cluster. Regions of Interest are available as output for the Level-2 trigger. Eight CP chips are necessary to fully process all the trigge r towers of one module.

Two streams of data are output from the CPM :

- Realtime data: multiplicity results of each CPM are sent through the backplane to two CMMs, which between them sum the total multiplicity for each of the 16 cluster thresholds over the 14 CPMs in each crate.
- Time-slice Data: on Level-1 Accept, DAQ and RoI data are formatted and sent to the ROD modules via a HP G-link

A full specification prototype CPM has been implemented on a 9U board and four of them have been manufactured. Intensive tests have been performed with the custom-built backplane. FPGA devices were loaded through flash memory via a VME interface. Stand-alone tests have been performed with data played back from local memories available on the board. Pseudo-physics data were sent and recovered correctly inside the CP chip, and the algorithm was checked to behave as specified. Data Source Sink (DSS) modules, designed earlier by the collaboration, have been used to send/receive signals to/from the CPM. Different flavours of daughter board mounted on the DSS enable us to investigate real-time and asynchronous data. A local TTC system was used to measure the timing limit of the board for the fastest parts. Bit Error Rate tests were performed on individual inputs to the level of 10^{-13}. The latency through the board has also been measured.

All tests were made by using the online ATLAS software framework. A C++ package has been developed to simulate expected data through the system, to help in debugging encoded information.

The CPM has been integrated with other boards of the Level-1 Calorimeter Trigger system. Timing limits of signals between CPMs and also from CPM to CMM were measured. Level-1 data from different boards were flagged and transferred to a ROD at a trigger rate up to 100 kHz.

All these tests show that the CPM design is successful and very few changes have to be made to the present layout for a production-ready final design.