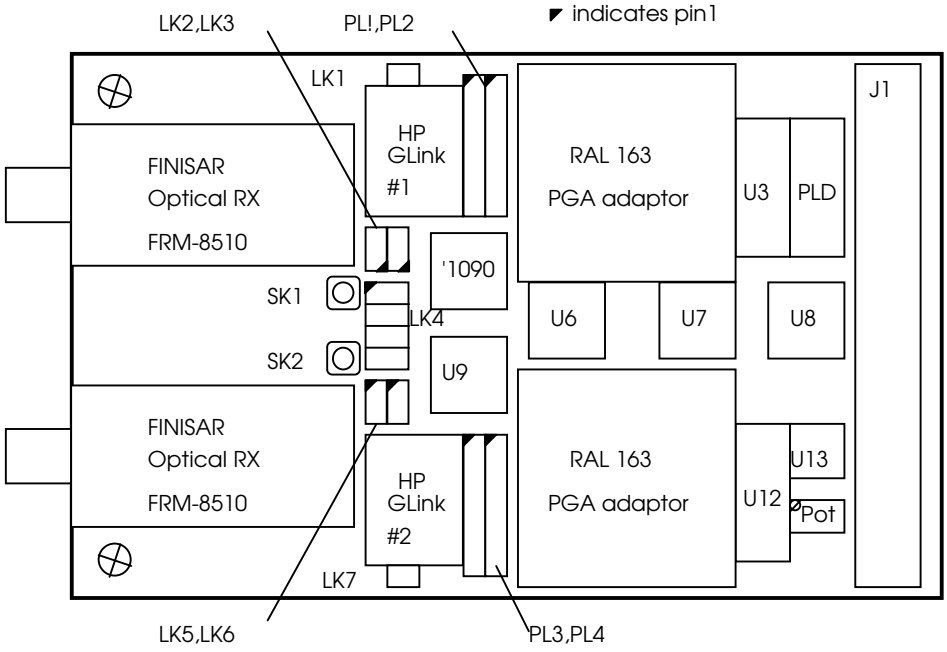
CPM GLink Daughter Card - User Guide 06/02/97

Features:

- Receive 2 High-speed serial GLink channels.
- Optical inputs via Finisar Rx Modules.
- Electrical inputs via SMB , A/C coupled or PECL levels, with or without cable equalisation.
- Status register for: Optical input signal level detection logic.
  Serial Number.(within PLD)
- GLink Error outputs and synchronisation control (via Motherboard.)

Layout:



Links:

LK1	GLink1: 1-2 M20SEL
LK2,LK3	GLink1 input source: 1-2 Electrical SK1, 2-3 Optical OC1
LK5,LK6	GLink2 input source: 1-2 Electrical SK2, 2-3 Optical OC2
LK4	GLink1 & GLink2: 4-8 EQEN, 3-7 FLGS, 2-6 DIV1, 1-5 DIV0
LK7	GLink2: 1-2 M20SEL
PL1,PL2	GLink1 16-bit data signals
PL3,PL4	GLink2 16-bit data signals

M20SEL	Link to Select 20bit data width. Otherwise 16bit data˝width.
EQEN	Link to Enable Cable equalisation. For electrical input.
FLGS	Link to use FLAG signal as extra data bit. Otherwise FLAG bit used for error detection.
DIV1,DIV0:	Glink VCO divider Select. Link = 1.

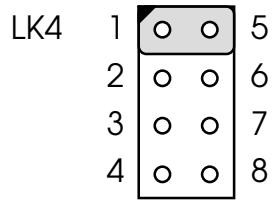
DIV1	DIV0	Word Rate MW/s
0	0	80 *1
0	1	40 *2
1	0	20 *3
1	1	10 *3

*1 For operation at 80MHz U6 must be fitted with a F100331 device, and the wires underneath removed.

*2 For operation at 40MHz U6 socket must be empty and the following pins underneath wired: **pin9 to pin 6** and **pin 19 to pin 3.**

*3 Not Used.

Default setting
(for 16bit transfers @ 40 MHz



The 'Pot' RV1 adjusts the reference voltage for the RAL ASICs' ECL inputs.
Pin 6 of U13 should be set at Vdd - 1.33V.

Memory Map, Onboard registers. Only lower 8 bits are active.

Address 0h : Serial number and board ID (from 1)
Address 2h : Status register,
- bit 0 Finisar 1 Signal Detect
- bit 1 Finisar 2 Signal Detect
- bit 2 Glink1 Ready
- bit 3 Glink2 Ready
- bit 4 EQEN link fitted

Address 100h- : P/S ASIC Error bits,
- bit 0 ASIC 1
- bit 1 ASIC 2

The160 locations above are associated with the 160 word memory within each ASIC.

R.Staley