Cluster Processor Module 2 Design Specification - Draft 06/02/97

VME Memory Map:

D16 , A24 standard and suppervisory addressing overall, with additional block transfer capabilities (BLT) and D32 for the memories.
Base address (upper 8 bits) set by two 'hex' switches.

Function	Access	Address Offset(hex.)	Size
Module I.D. register	RO	0	1 Word
Control register	R/W	2	1 Word
Status register	RO	4	1 Word
GLINK Reset reg.	R/W	6	1 Word
GLink Error Count	R/O	8	1 Word
GLink Error-bit Timing	R/W	A	1 Word
Software clocks	WO	C	1 Word
Timeslice Counter	RO	10	1 Word
Cluster ASIC thresholds	R/W	20-	4 x 4 Words
Fine Delay registers	R/W	40-	13 Words
Daughter Card	R/W	1000-	2048 Words
Serial/Parallel ASICs	R/W	2000-	13 x 128 Words
Parallel/Serial ASICs	R/W	2E00-	2 x 128 Words
Output Memory	R/W	3000-	4 x 256 Words, +D32
Output Memory	R/W	3800-	4 x 256 Words, +D32
Input Memory	R/W	4000-	25 x 256 Bytes, +D32
Input Memory	R/W	6000-	25 x 256 Bytes, +D32

R/W = Read and Write, RO = Read only, WO = Write only.
+D32 = 32bit data access, as well as 16bit..

Module I.D. reg.(RO)

Bits 15-11	Type number. For the CPM this is '3'
Bits 10-8	Revision number (from 1)
Bits 7-0	Serial number (from 1), Bits 5-0 are set by external links.

Control register (R/W)

Bit 0	RAM access	1=VME access, 0=DAQ .
Bit 1	Clear VME error	1=Clear VME Error Flag.(pulsed)
Bit 2	Pipeline Run	1=Clear 'Stop' Flag (pulsed)
Bit 3	PLL Clock Test	1=Software access. 0=Normal Operation.
Bit 5	Pipeline Stop	1=Active. ORed with external 'Stop' signal.(pulsed)
Bit 7	ASIC Reset	1=Reset CP and S/P ASICs. 0=Normal Operation.

Bits 4,6 and 8-15 are present but have no function except for write-readback testing.

Status Register (RO)

Bit 0	Stop Flag	Set by external Stop signal. Hold Timeslice counter. Cleared by Control Register bit 2.
Bit 1	VME Error Flag	Set if VME access to barred RAM Cleared by Control Register bit 1.
Bit 2	40MHz Clock	1=Present
Bit 3	Subsidiary Clock	1=Present

GLink Error Count (RO)

Bits 0-7	GLink 0 error count
Bits 8-15	GLink 1 error count

(see also Output Memory)

GLINK / Daughter Card Reset reg. (R/W)

Bit 0	P/S ASIC	1=Reset. 0=Normal Operation
Bit 1	GLink Synchronisation	1=Reset. 0=Normal Operation
Bit 2	GLink Error Counters	1=Clear.(pulsed)

GLink Error Bit Timing (R/W)

Bit 0	GLink0 timing adjust:	0=Sample on rising edge of system clock.
Bit 1	GLink1 timing adjust:	1=Sample on falling edge of system clock.

Software Clocks (WO)

Enabled by 'PLL Test' of control register.

Bit 0	PLL clock	1=Pulse
	Pulse PLL clock distribution network driving S/P ASICs,	
	160MHz clock line cycles every 32 pulses, 40MHz cycles every 128 pulses.	
Bit 1	Memory/Counter clocks	1=Pulse
	Pulse memory counters , memory write (if enabled) and CP ASIC .	

Timeslice Counter (RO)

Bits 0 - 7 8-bit pointer for Input and Output Memories

S/P ASIC Clock Fine Delay register (R/W)

Bits 0-4 Delay in 0.25ns increments, 0 to 7.75ns. Values ≥ 4ns are not recomended.

Address +0	ASIC0	Address +E	ASIC7
Address +2	ASIC1	Address +10	ASIC8
Address +4	ASIC2	Address +12	ASIC9
Address +6	ASIC3	Address +14	ASIC10
Address +8	ASIC4	Address +16	ASIC11
Address +A	ASIC5	Address +18	ASIC12
Address +C	ASIC6		

Daughter Card

16 bit data , 8bit address area for use by daughter card. The Parallel-to-Serial ASICs have their own address area that is separate from other items on the daughter card.

For the Glink Daughter card:

Address + 0	**Serial number (RO).**
Address + 2	**Status register (RO).**
	Bit 0 Finisar Optics' "Signal Detect" output link1
	Bit 1 Finisar Optics' "Signal Detect" output link2
	Bit 2 GLink Ready, link1
	Bit 3 GLink Ready, link2
	Bit 4 Glink EQEN set (input signal equaliser selected)
Address + 100h -	**P/S ASIC Memory error / 17th data bit (RO).**
	Bit 0 ASIC0 error bit
	Bit 1 ASIC1 error bit

Serial to Parallel ASICs (R/W) Bits15-0
The internal ASIC memories , when used in this mode, have no external function, ie they cannot record or playback data.

Address +0	S/P ASIC 0	(Cells 11 & 21)
Address +100h	S/P ASIC 1	(Cells 31 & 41)
Address +200h	S/P ASIC 2	(Cells 51 & 12)
Address +300h	S/P ASIC 3	(Cells 22 & 32)
Address +400h	S/P ASIC 4	(Cells 42 & 52)
Address +500h	S/P ASIC 5	(Cells 13)
Address +600h	S/P ASIC 6	(Cells 23 & 33)
Address +700h	S/P ASIC 7	(Cells 43 & 53)
Address +800h	S/P ASIC 8	(Cells 14 & 24)
Address +900h	S/P ASIC 9	(Cells 34 & 44)
Address +A00h	S/P ASIC 10	(Cells 54 & 15)
Address +B00h	S/P ASIC 11	(Cells 25 & 35)
Address +C00h	S/P ASIC 12	(Cells 45 & 55)

With each ASIC structure appearing as:

Address +0 to +9Eh	Memory
Address +A0h	Control Register
Address +A2h	Test Register

Parallel to Serial ASICs (R/W) Bits15-0
The error bits (17th data bit) from both ASICs are available via locations within the Daughter Card address range.

Address +E00h	P/S ASIC 0	(Cells 22 & 32)
Address +F00h	P/S ASIC 1	(Cells 23 & 33)

Cluster ASIC Thresholds (R/W)

Address + 0h	CF ASIC0	(Ref Cell 22)	
Address + 8h	CF ASIC1	(Ref Cell 32)	
Address + 10h	CF ASIC2	(Ref Cell 23)	
Address + 18h	CF ASIC3	(Ref Cell 33)	

With each ASIC structure appearing as:

Address + 0h	Cluster threshold 1	9 bits	D0-D8
Address + 2h	Cluster threshold 2	9 bits	D0-D8
Address + 4h	Isolation threshold 1	12 bits	D0-D11
Address + 6h	Isolation threshold 2	12 bits	D0-D11

Input Memory (R/W)

Grouped into timeslots:

Address + 00h to + 1Fh Timeslot 0
Address + 20h to + 3Fh Timeslot 1
.....
Address +1FE0h to +1FFFh Timeslot 255

Each timeslot has the following address structure, for a 32 bit read:
Each cell is 8 bits of data.

Timeslot N	D31-D24	D23-D16	D15-D8	D7-D0
Address +0h	Cell 11	Cell 21	Cell 31	Cell 41
+4h	Cell 51	Cell 12	Cell 22	Cell 32
+8h	Cell 42	Cell 52	Cell 13	Cell 23
+Ch	Cell 33	Cell 43	Cell 53	Cell 14
+10h	Cell 24	Cell 34	Cell 44	Cell 54
+14h	Cell 15	Cell 25	Cell 35	Cell 45
+18h	Cell 55			
+1Ch				

Output Memory (R/W)

Grouped into timeslots:

Address +0 to 7 Timeslot 0
Address +8 to Fh Timeslot 1
.....
Address +7F8h to 7FFh Timeslot 255

where each timeslot has the following structure:

		MSB				LSB
Address +0	ASIC0	Err2	Err1	Hit2	Hit1	12bit Sum
Address +2	ASIC1	0	0	Hit2	Hit1	12bit Sum
Address +4	ASIC2	0	0	Hit2	Hit1	12bit Sum
Address +6	ASIC3	0	0	Hit2	Hit1	12bit Sum

Hit2,Hit1 and the 12bit Sum are from the respective CP ASIC.
Err2 and Err1 originate from the GLink Devices but are captured by the spare bits of this memory to avoid adding extra components.