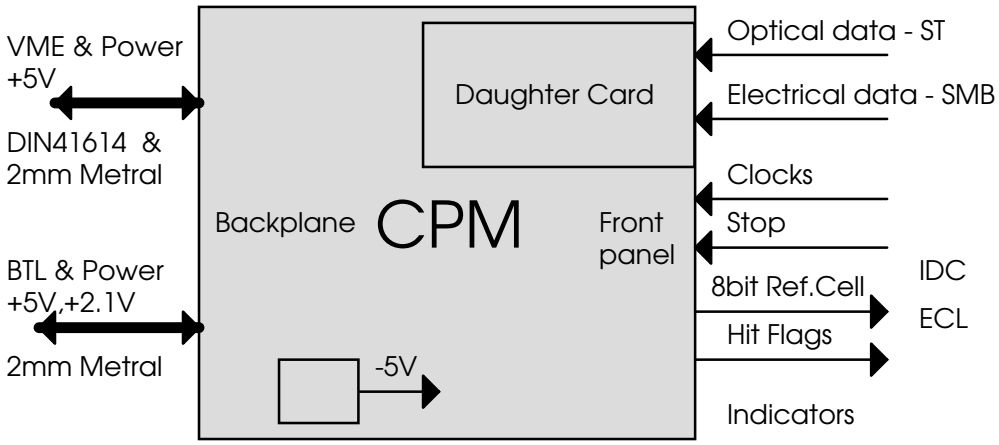
Introduction

The module processes 8 bit data from an array of 5x5 trigger cells arriving every 25ns. The data enters a module over two high speed serial links, each carrying data from two trigger cells. These cells are processed on-board and also exchanged with other modules via the backplane. Across the backplane, each trigger cell is multiplexed onto two lines in order to reduce the number of pins needed on the backplane connector.The 4 trigger cells arriving via the front panel serial links are fanned-out to adjacent modules. The remaining 21 cell needed to complete the 5x5 array arrive via the backplane.

The 'Serial to multiplexing' function is performed by a multi-chip module and the demultiplexing function by an ASIC. The processing is performed every 25ns by a group of four 'Phase 1' Cluster Processing ASICs.



Features

VME Access, A24,D16 with D32 for memory. Module Base Address is switch selectable to any 64K boundary, within the 16MByte A24 address space. The memory area also support block transfers.

The memories located at the inputs and outputs of the Cluster Processing ASIC. These are filled in a cyclic manner, but appear to the VME bus as a linear sequence of time slots.
Memory access barred during data capture. An Error Flag will be set in status reg. to indicate this. (BERR will not be activated, the cycle will complete as normal with DTACK)

Control register is read-write.

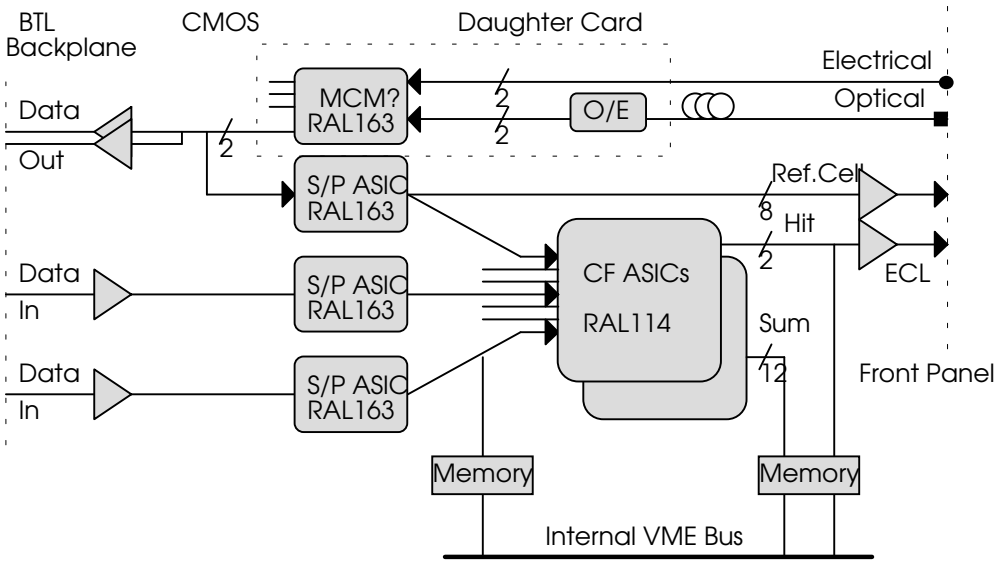
Module identification register.

Timeslice counter is 256 slices deep.

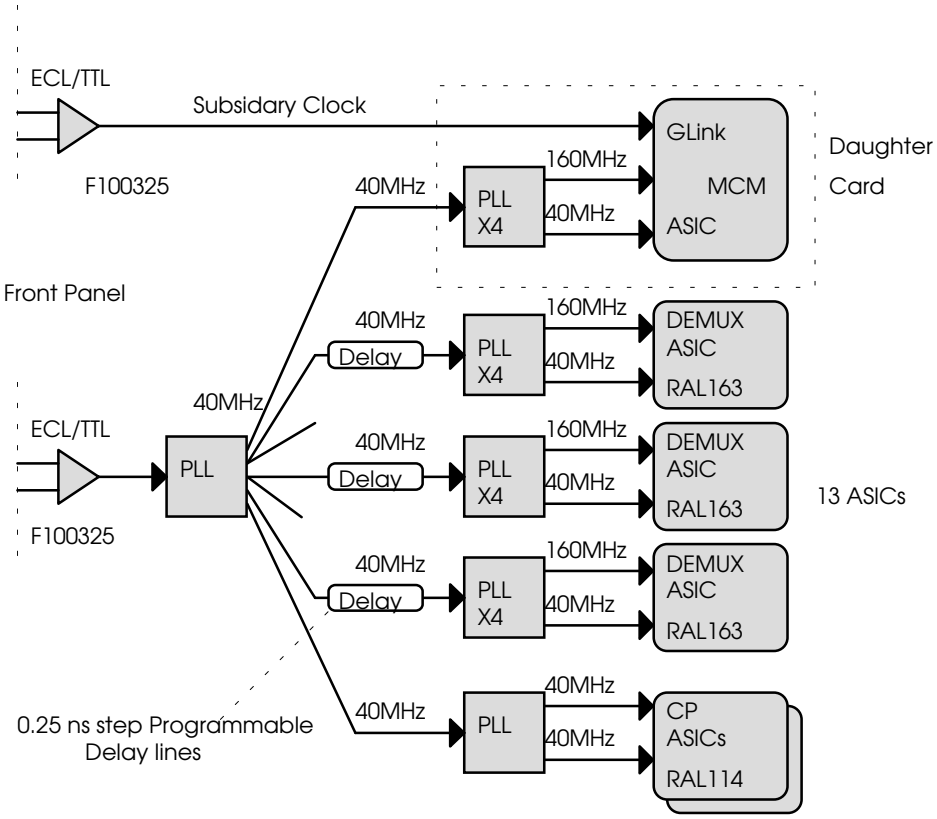
Error Flags and counters for HP links.

The module will tolerate up to 10% variation in the frequency of the 40MHz system clock.

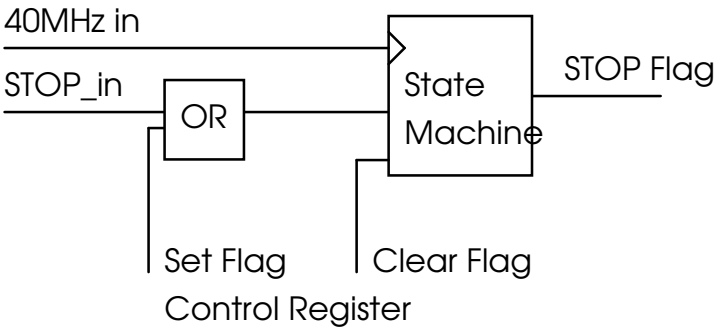
Module Block diagram (Showing Data Path):



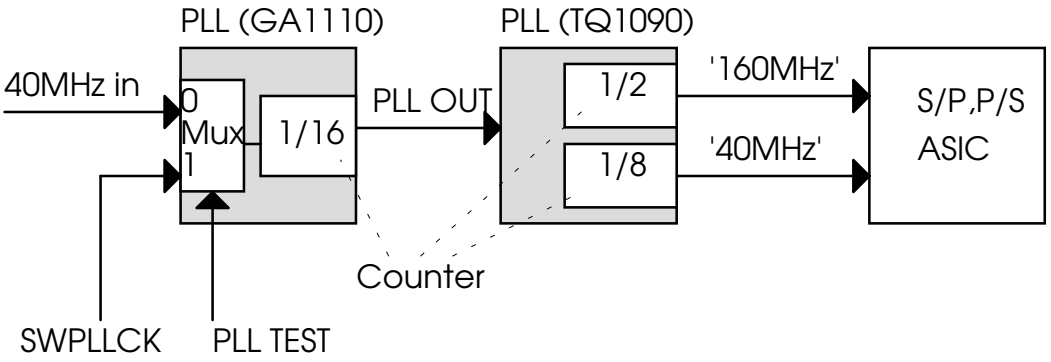
Clock Distribution:



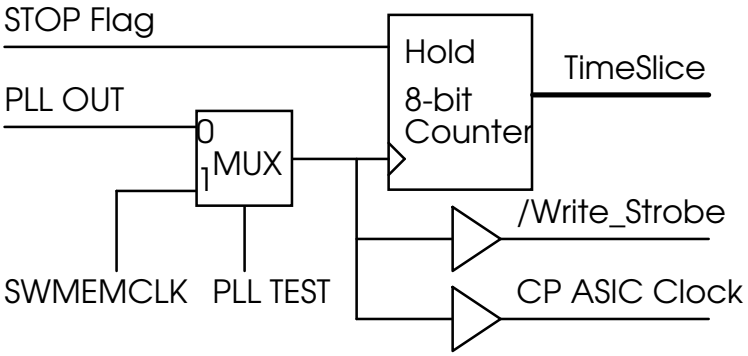
Pipeline Stop Logic



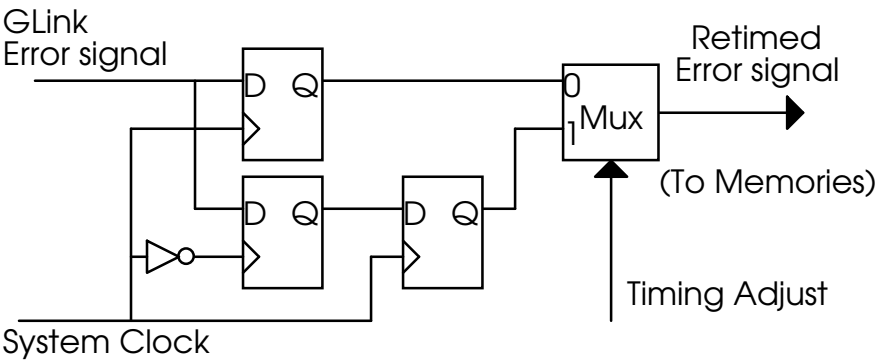
Test Access to S/P ASIC clock signals



Test Access to CP ASIC clock and Memory signals



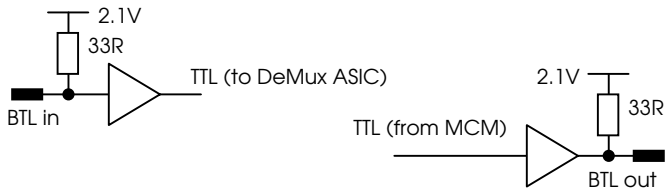
GLink Error Signal Timing



Interfaces:

1)Fast Backplane, 160MHz BTL.

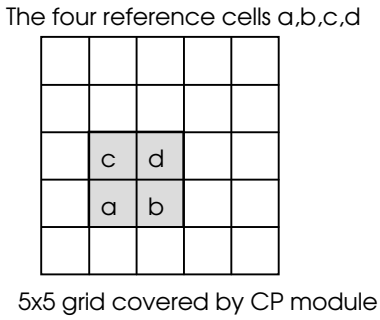
The fast backplane is driven with the Nationals BTL family. The connections are point-to-point links with terminators located on-board at receivers. Termination is to +2.1V by 33Ω. The connector is a 2mm 48 x 4 pin Futurebus+ type.

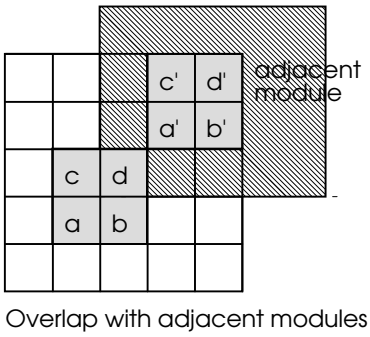


TheModule drives 21signal pairs @ 160Mb/s onto the backplane and receives 21signal pairs @ 160Mb/s from the backplane.
Each signal pair represents the data from a single trigger cell arriving every 25ns.
The driven signals originate from the Module's 4 reference cells being fanned out electrically as appropriate.
The dimensions are in accordance with DIN41494 part5 and IEEE P1596.

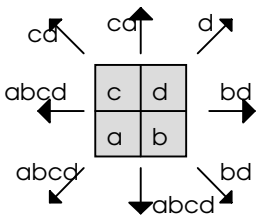
CPM - Backplane/ Module Fan-out

Each module receives 4 trigger cells via the serial links. As well as being used onboard, they are also fanned out to adjacent modules. These 4 cells are also the 4 reference cells of the 5x5 grid. the remaining 21 cells come in over the backplane from adjacent modules.





These 4 cells interconnect with the other 8 adjacent modules as follows, (by sliding the 5x5 grid 2 places in either or both directions.)



Thus the fanout for a particular cell is:

a	**3**
b	**5**
c	**5**
d	**8**
Total	**21 cells**

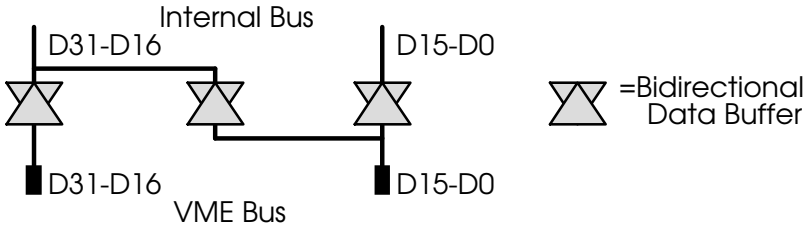
= 42 signals driven onto the backplane.

The cell numbering scheme within the module will be of the form x,y, starting from 1,1 up to 5,5.

2)Control Bus, VME.

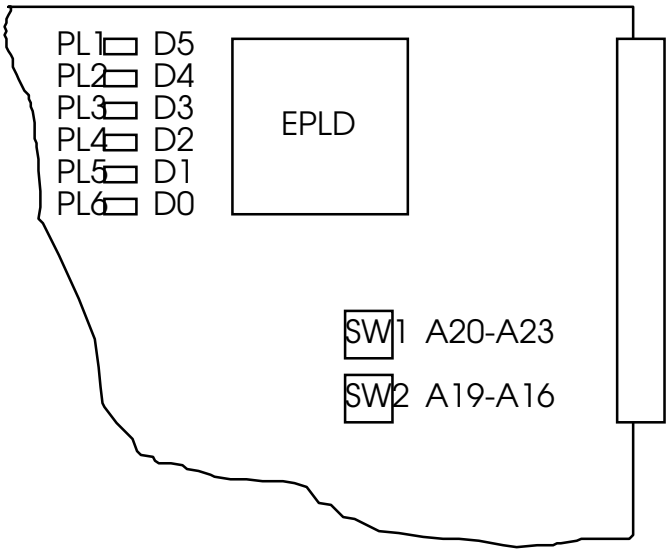
The control bus consists of a standard VME J1 connector plus a non-standard 2mm 12x4 Futurebus+ type connector carrying the VME J2 signals. Elseware in the crate is a transition 'unit' that allows standard VME boards (such as VIP) to be connected into the system.

Data Path Routing- For 32Bit or 16Bit VME Bus transfers:
The internal memory data bus is 32 bits wide, with routing to allow 16bit wide VME transfers:



The internal Control and Status bus is 16bits wide.

Links & Switches



PL1-6 Encode the serial number. A link present = logic 1

SW1-2 Set the VME base address of the card , indicated in hexadecimal.
SW1 is the MSD:

A23-A20	A19-A16	A15-A12	A11-A8	A7-A4	A3-A1
SW1	SW2	X	X	X	X

3)Front panel signals; 800Mb/s High-speed serial:

2 Electrical for G-link	SMB co-axial connectors
2 Optical for Finisar recevers.	ST type Bulkhead connectors

4)Front panel signals; 40Mb/s:

All signals on J4,J5,J6 & J7 are differential 100K ECL.

Timing values taken from manufactures data sheets, commercial operating range:
0 - 70 °C , Vcc and Vee Supplies +/-10%
Where appropriate, times refer to the rising(active) edge of Clock-in.

J4 - Reference Cells and Clock Outputs

40 Mhz Clock	Pin34	-	+	Pin33
Cell32 bit7	Pin32	-	+	Pin31
Cell32 bit6	Pin30	-	+	
Cell32 bit5		-	+	
Cell32 bit4		-	+	
Cell32 bit3		-	+	
Cell32 bit2		-	+	
Cell32 bit1		-	+	
Cell32 bit0		-	+	
Cell22 bit7		-	+	
Cell22 bit6		-	+	
Cell22 bit5		-	+	
Cell22 bit4		-	+	
Cell22 bit3		-	+	
Cell22 bit2		-	+	
Cell22 bit1		-	+	
Cell22 bit0	Pin2	-	+	Pin1

J5 - Reference Cells and Clock Outputs

40 Mhz Clock	Pin34	-	+	Pin33
Cell33 bit7	Pin32	-	+	Pin31
Cell33 bit6	Pin30	-	+	
Cell33 bit5		-	+	
Cell33 bit4		-	+	
Cell33 bit3		-	+	
Cell33 bit2		-	+	
Cell33 bit1		-	+	
Cell33 bit0		-	+	
Cell23 bit7		-	+	
Cell23 bit6		-	+	
Cell23 bit5		-	+	
Cell23 bit4		-	+	
Cell23 bit3		-	+	
Cell23 bit2		-	+	
Cell23 bit1		-	+	
Cell23 bit0	Pin2	-	+	Pin1

Timing performance

Cell outputs from 40MHz clock-in	t_{CO}min = 14ns , t_{CO}max = 22ns
Clock output from 40MHz clock-in	t_{PD}min = 1.4ns , t_{PD}max = 6.6ns

J6 - CP ASIC Hit Outputs

ΣHit2(OR)	Pin20	-	+	Pin19
ΣHit1 (OR)	Pin18	-	+	Pin17
ASIC3 Hit2	Pin16	-	+	Pin15
ASIC3 Hit1	Pin14	-	+	Pin13
ASIC2 Hit2	Pin12	-	+	Pin11
ASIC2 Hit1	Pin10	-	+	Pin9
ASIC1 Hit2	Pin8	-	+	Pin7
ASIC1 Hit1	Pin6	-	+	Pin5
ASIC0 Hit2	Pin 4	-	+	Pin3
ASIC0 Hit1	Pin 2	-	+	Pin1

Timing performance:

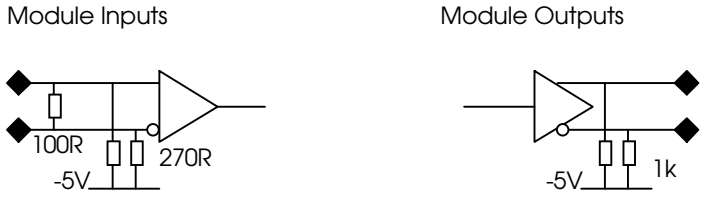
CP ASIC Hit outputs from 40MHz clock t_{CO}min = 4ns , t_{CO}max = 18ns

J7 - Clock and Control inputs

	Pin10			Pin9
	Pin 8			Pin7
Stop in	Pin 6	-	+	Pin5
Subsidiary Clock in	Pin 4	-	+	Pin3
40MHz Clock in	Pin 2	-	+	Pin1

Timing requirements

40MHz Clock Frequency Fck	Between 36MHz and 44MHz (10%)
Subsidiary Clock Frequency	Offset from Fck by between 0.1% and 0.001%.
Stop Signal to 40MHz Clock-in	t_{SETUP} = 13ns , t_{HOLD} = 1ns



Typical characteristics for the ECL input devices are:

Minimum differential signal: 150mV

Common mode range: -2.0V to -0.5V

Typical characteristics for the ECL output devices are:

Logic high: -0.95V

Logic low: -1.70V

5)Front panel Indicators

From top to bottom:

+5v Power.	Green	
+2.1v Power.	Green	
-5v Power.	Green	
VME Access.	Amber	(Flash)
VME Error	Red	(Flash)
STOP	Amber	(While Pipeline stopped)
GLINK Errors.	Red	(While Error Count ≠ 0)
40M Clock	Green	(When present)
Sub Clock	Green	(When present)

VME Memory Map:

D16 , A24 standard and suppervisory addressing overall, with additional block transfer capabilities (BLT) and D32 for the memories.
Base address (upper 8 bits) set by two 'hex' switches.

Function	Access	Address Offset(hex.)	Size
Module I.D. register	RO	0	1 Word
Control register	R/W	2	1 Word
Status register	RO	4	1 Word
GLINK Reset reg.	R/W	6	1 Word
GLink Error Count	R/O	8	1 Word
GLink Error-bit Timing	R/W	A	1 Word
Software clocks	R/W	C	1 Word
Timeslice Counter	RO	10	1 Word
Cluster ASIC thresholds	R/W	20-	4 x 4 Words
Fine Delay registers	R/W	40-	13 Words
Daughter Card	R/W	1000-	2048 Words
Serial/Parallel ASICs	R/W	2000-	13 x 128 Words
Parallel/Serial ASICs	R/W	2E00-	2 x 128 Words
Output Memory	R/W	3000-	4 x 256 Words, +D32
Output Memory	R/W	3800-	4 x 256 Words, +D32
Input Memory	R/W	4000-	25 x 256 Bytes, +D32
Input Memory	R/W	6000-	25 x 256 Bytes, +D32

R/W = Read and Write, RO = Read only.
+D32 = 32bit data access, as well as 16bit..

CPM - Circuit description **Draft** **06/02/97**
With reference to RAL schematics PC3060M

Sheet 1 CP ASICs.

Cell signals are numbered 'Cell xy'. ASIC symbol gives numbering as 'Eyx'.
ASIC inputs E32 and E33 exchanged, compensating for ASIC˝ error.

Sheet 2 & Sheet 3 Input Memory.

Memory inputs come directly from S/P ASICs. Memories also connected via buffers to internal 32bit Data Bus. Memory addresses are selected from either timeslice counter or the internal Address bus using the READOUT signal from the control register. A number of multiplexers are used to fan-out the address signals to the 25 memory cells. Multiplexers are also used to select and fanout the memory write signals.
Two write signals, HIWRn and LOWRn , allow 16bit write operations, and memory CMCSn and buffer CBENn signals select which bank is to be accessed. During DAQ all memory WE and CE signals are active.

Sheet 4 Output Memory.

As for Input Memory with addition of a buffer , to disconnect the CPASIC output from the memory during a VME access.

Sheet 5 BTL Drivers and Receivers.

The BTL drivers perform a fan-out of up to 8 ways. Driver inputs are terminated to +2V, and outputs' have an optional pull-up resistor. Receiver inputs from the backplane are terminated. The terminating resistors for the Receiver outputs are located at the S/P ASICs.

Sheet 6 ECL I/O.

The four reference cells are driven out in parallel, together with a suitable clock. Pull-downs on the outputs allow monitoring with an oscilloscope.
Individual HIT outputs from each CPASIC will also be ORed together.
The 16V8 PAL generates the 'STOP' flag.
A DC/DC converter generates -5V for the ECL parts.

Sheet 7 VME interface.

A 20V8 PAL provides Address Modifier selection and block transfer logic. A comparator (74F521) on the upper address lines also feeds this PAL. A register (74F377) and counter latch the VME addresses for internal use.
Six Data buffers route the internal 32bit Data bus as necessary , for either 16bit or 32bit transfers.
One EPLD(Address EPLD), with delay lines, performs Address decoding and DTACK timing .
Another EPLD(Control EPLD) contains the ID, control and status registers, error counters and a serial interface controller for delay lines.

Sheet 8 Serial to Parallel ASICs.

Sheet 9 Clock distribution.

Delay lines, with sub-nanosecond resolution, feed 40MHz clock to PLLs which regenerate this clock, and also a 160MHz clock for the S/P ASICs. The regenerated clocks are held precisely in phase with the 40MHz clock, to compensate for the poor timing margins imposed by the BTL transceivers.
The delay lines will be/are controlled using a serial link.

Sheet 10 J3 Connectors , LED drivers and Clock drivers.

Signals Gerror, 40MPres and SubPres originate from within the Control EPLD.
/BDENAB from VME selection logic , and ACCERR from Address EPLD.
Also on this sheet are the module's 40MHz Clock driver (PLL) and memory 'write pulse' circuitry.