Central Trigger Processor Demonstrator

(CTPD)

RD27 Project

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Abstract:

The Level-1 Central Trigger Processors (CTP) forms the final Level-1 trigger decision from sub-detectors trigger data (calorimeter, muon,...). It makes a decision every bunch crossing and may therefore be seen as a fully synchronous 40 MHz processor. The current demonstrator is a reduced version of the CTP as it looks at only 32 inputs (instead of 128) and implements only 32 level-1 conditions (instead of 96). It has been built to acquire experience and validate choices (architecture, use of FPGAs, latency time,...) and to allow the use of sub-detectors level-1 capability in beam tests.

Rev 0 Aug. 96

Specifications.

Mechanical standard.

9U VME module, single width. J1, J2 and JAUX required [1]

VME capabilities.

A32/D32 slave. AM codes: $09, 0D, 0B, 0F.

Signal levels on coaxial connectors.

NIM (-16 mA in 50 Ω)

Signal levels on differential connectors.

Input: ECL differential; input impedance 50 Ω.

Output: ECL differential. Pull down resistor 100 Ω @ -2V.

Total latency.

2.5 Clock periods @ 40 MHz.

Power consumption @ nominal frequency.

xxxA @ 5V.

yyyA @ -5.2V.

Total power: zzzW.

1. General Description.

1.1. Introduction.

The CTPD receives up to 32 inputs from the sub-detectors level-1 processors. These inputs are grouped in 8 sets of 4 signals, each of them being accompanied by its synchronisation clock.
The first task of the module consists of synchronising these sets of signals with the internal module clock and equalising the latencies introduced by the different sub-detector level-1 systems so that the 32 signals corresponding to one bunch crossing are aligned before the decision is made.
The second task consists of making a decision (level-1 accept or reject). Out of the 2^{32} possible input combinations, 32 level-1 accept combinations are selected, providing 32 internal Level-1 Accept (L1A) signals. These signals can then be masked or prescaled before the final L1A signal is generated.
Additional control and monitoring functions are implemented as well as read-out capability.

1.2. Block diagram of the CTPD.

The CTPD block diagram is given in fig. 1. It consists of 12 main blocks.
The 8 groups of 4 inputs (differential ECL) are first translated to TTL level in the block IOCON before being presented to the VLP block in charge of the synchronisation with the internal clock (BC0) and of the alignment. The 8 differential ECL signals associated with each group (SDC) are presented to the block TDC which measures the phase difference with BC0 and gives the proper clock signals (BC0 or BC1) used to strobe the inputs.
At the output of the VLP block, the bit pattern (PIT) belongs to the same physical beam crossing and is presented to the look-up table (LMV block). It is also loaded in a FiFo of the RDOUT block for a later VME read-out. The block CNTS contains counters which count the occurrence of each bit of the PIT. These counter can be read-out in order to do monitoring.
The output TBV of the look-up table is a 32 bit pattern. Each bit of this pattern indicates that one predetermined combination (out of the 2^{32}) has been detected and that we

have a potential level-1 candidate. Each bit of this pattern is also counted in the block CNTS.
These 32 level-1 candidates are then gated with 32 individual VETOs, a global external VETO and a dead-time signal which is a combination of TAP, GDT1 and GDT2. The output of this stage gives another 32 bit pattern (TAV) which are loaded in a FiFo for later VME read-out. They are also prescaled in programmable prescalers of the PRES block.

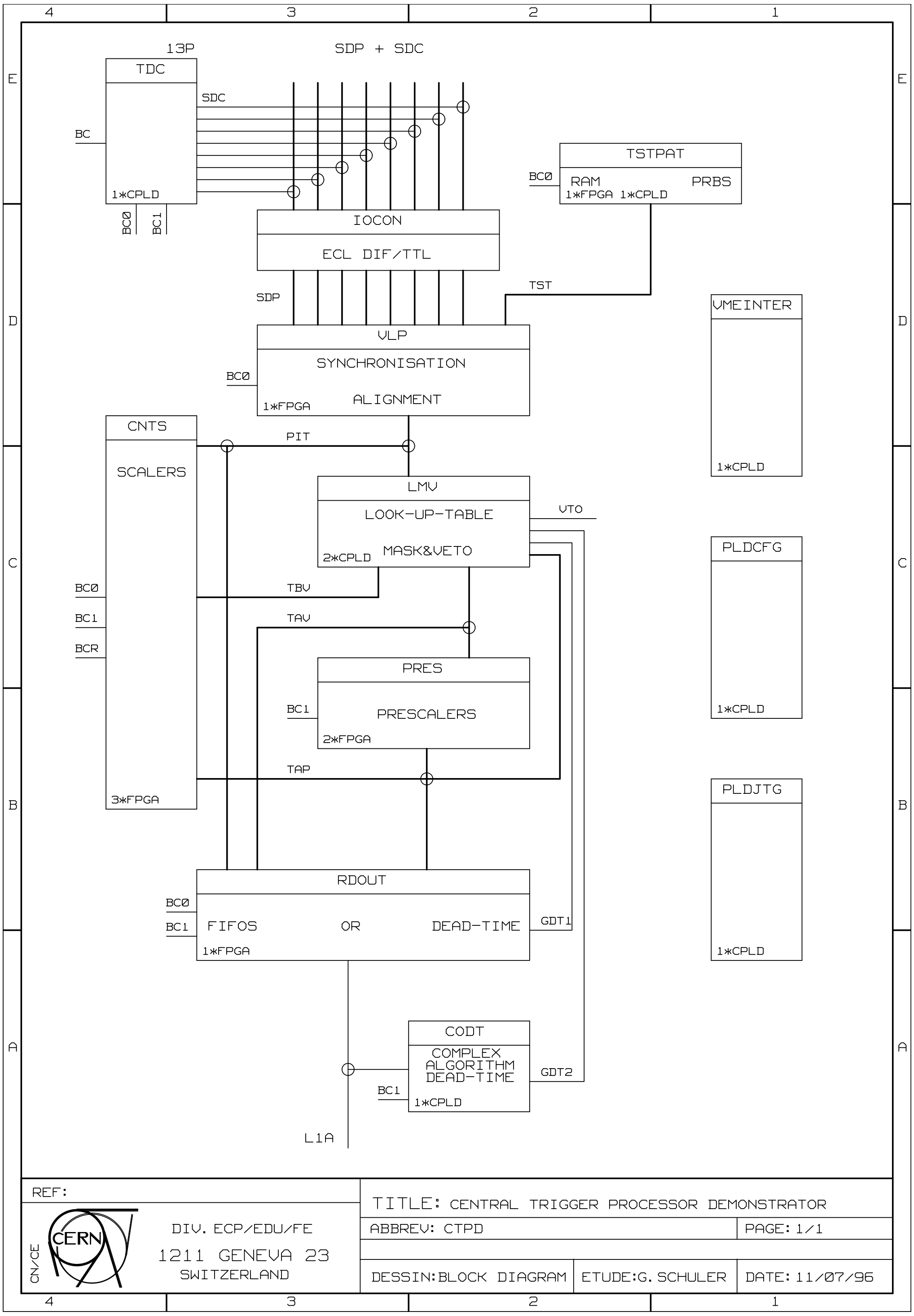


Fig.1. CTPD Block Diagram.

After this last filtering stage the 32 level-1 accept candidates are counted in the CNTS block, loaded in a FiFo of the RDOUT block and a global OR of these signals gives the L1A signal.
The other blocks are used for test, control and configuration purposes.

The TSTPAT block gives 32 bit patterns (TST) which can be used instead of the SDP inputs. These patterns are coming from a memory where they have been written or from a pseudo random generator.
The VMEINTER block contains the VME slave interface of the module.
The PLDCFG block takes care of the configuration (programmation) of the in-situ programmable FPGAs. At power up or when a new configuration is needed the memory content of this block (written through VME) is loaded in the FPGAs.
The PLDJTG block controls the JTAG chain which connects most of the ICs of the module. This chain will allow to make boundary scan tests and also in the future to configure the FPGAs.

1.3. Design description.

The 12 functional blocks of the CTPD are described in this section.

1.3.1. IOCON block.

The level conversion of the input and output signals are made in this block:

- XSDP<31..0> and XSDPN<31..0>
    - bit pattern coming from the sub-detectors level-1 processors
    - differential ECL inputs
    - front panel connector type xxxxx
    - 51 Ω to -2V termination
    - TTL translation with 10H125.
- XBC_N
    - LHC clock
    - NIM level
    - front panel connector type xxxxx
    - 51 Ω to ground termination
    - AC coupled
    - ECL translation with 10E416
- XBC_E and XBCN_E
    - LHC clock
    - differential ECL level
    - front panel connector type xxxxx
    - 51 Ω to -2V termination
    - AC coupled
    - ECL regeneration with 10E416
- XVTON_N
    - Global veto signal

    - NIM level
    - front panel connector type xxxxx
    - 51 Ω to ground termination
    - ECL translation with 10E416 and TTL Translation with 10ELT25
- XBCRN_N
    - Bunch counter reset signal coming from TTC
    - NIM level
    - front panel connector type xxxxx
    - 51 Ω to ground termination
    - ECL translation with 10E416 and TTL translation with 10ELT25
- L1A_E and L1AN_E
    - Level-1 accept signal
    - ECL differential output
    - front panel connector type xxxxx
    - issued by a 10ELT24 with pull down resistors 100 Ω to -2V
- L1A_N
    - Level-1 accept signal
    - NIM level output
    - front panel connector type xxxxx
    - issued by a TTL/ECL translator (10ELT24) and a pair of transistors
    - level limitation to 2 diode thresholds

1.3.2. VLP block

This block takes care of the synchronisation with the internal clock and of the alignment of the incoming data (compensation of the latency differences of level-1 processing in different sub-detectors). It mainly consists of flip-flops.

The synchronisation assumes that the input signals jitter is small and that their phase is stable. The phase of the timing signal SDC coming with the data and the data (SDP) must be known and stable. The phase of the 8 timing signals with respect to the internal clock BC0 is measured. Depending on the result of the measurement, BC0 or it’s complement is used to strobe the inputs (fig.2).

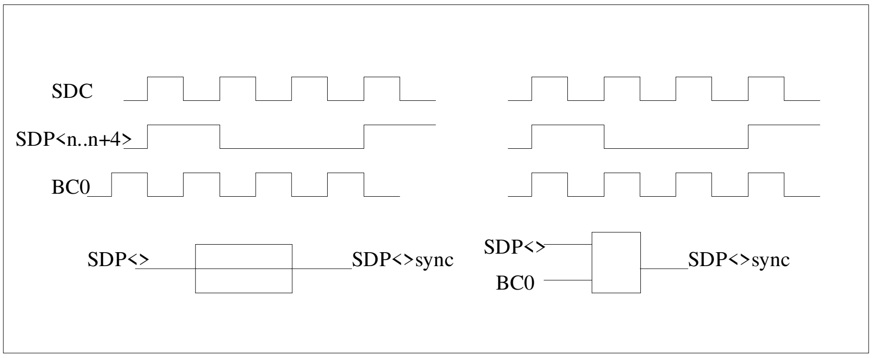


Fig. 2. Input synchronisation.

Once synchronised each group of inputs is delayed by the ad-hoc number of clock cycles in order to compensate for the different latency in the sub-detectors level-1 processors. This is done by means of shift registers as shown on fig. 3.

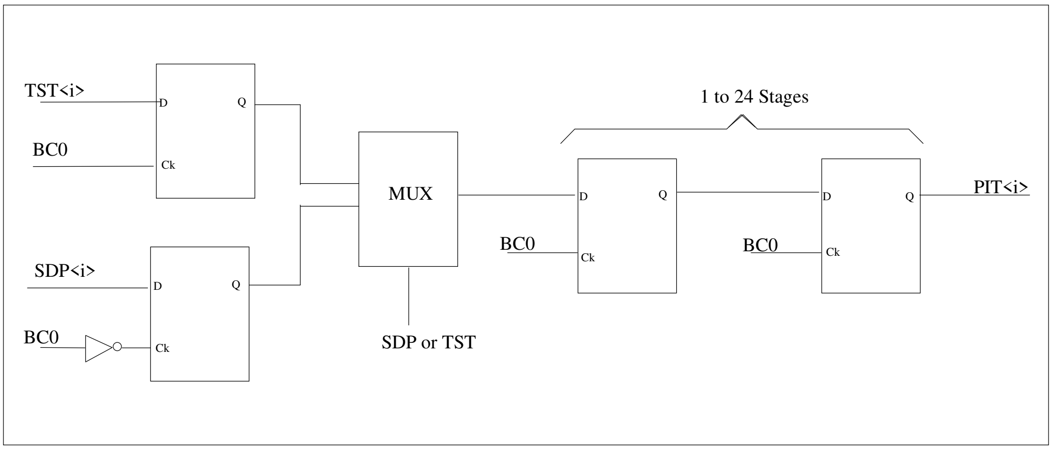


Fig. 3. Synchronisation and alignment.

The synchronisation and alignment tasks are performed in an in situ programmable FPGA (EPF81500ARC240-2). Insertion of synchronisation flip-flops and length of the alignment shift registers can then be configured in situ. It's nonetheless not a simple operation as a change of configuration requires a recompilation of the FPGA source file with proprietary software (Maxplus from Altera). It's assumed that this operation needs not be done very often (hopefully the different latencies of each sub-detector level-1 electronics is constant). It has been checked that any shift register length (from 1 to 24) can be implemented in this FPGA.

The performances of this circuitry are:

- Set-up time SDP/BC0 : 0 ns.
- Propagation delay PIT<i>/BC0 : 12.1 ns.
- Latency from 1 to 24.5 Clock cycles.

1.3.3. TDC block

This block contains the necessary circuitry to:

- measure the phase of the incoming timing signals with respect to the internal clock.
- generate, select, position and fan-out the internal clock.
- measure the module temperature.
- measure the power voltages.

1.3.3.1. Phase measurement.

The signal to be measured is selectable. It could be:

- One of the 8 timing signals SDC<7..0> and SDCN<7..0> coming with each group of 4 bits SDP. These signals come from the input connector.
- The global veto signal VTO.
- The bunch counter reset signal BCR.

The selection is made through differential multiplexers (10EL57), a level translator (10H600) and a few cells of a CPLD referenced TDCC in the schematic (EPM7128EQC160-10P). The content of a VME accessible register at the address Base+$61 defines the selection:

Data	Selected signal
$20	SDC0
$21	SDC1
$22	SDC2
$23	SDC3
$30	SDC4
$34	SDC5
$38	SDC6
$3C	SDC7
$00	VTO
$10	BCR

The selected signal is sent to 2 phase measurement circuits:

- One gives an immediate phase measurement with a resolution of ± 2.5 ns. It uses a vernier principle and is made with a 25 ns delay line with intermediate outputs each 5 ns (EL511-25), a 5 bit register (10E151), a level translator (10H601) and a few cells of the CPLD TDCC.
  The 5 bit measurement result is readable at VME address Base+$64. Value 0 means in phase signals.

- The other one gives an average measurement of the phase. It only works for the SDC signals (neither for BCR nor for VTO). It uses a phase comparator (MCH12140), an integrator (RC) and an 8 bit ADC (MAX155BCWI). The 8 bit measurement result is accessible at VME address BASE+$63 after having requested a conversion with a write at the address Base+$E0.

Important remarks:

1. The read value is valid only after the second conversion.
2. The conversion duration is 4,5 µs. During that time no VME Dtack is given.
3. The sensitivity is about 1.8 LSB per ns. Value 0 means that signals are in phase.

1.3.3.2. Internal clocks generation.

The internal clock of the module can be:

- An internal 40 MHz clock (quartz 80 MHz RED6200A and divider by 2 10EL34).
- An internal 10 MHz clock (same quartz and a divider by 8).
- The external NIM input clock XBC_N.
- The external differential ECL input clock XBC_E and XBCN_E.

The selection between these 4 sources is done with a multiplexer (100EL57), a level translator and a few macro-cells of the CPLD TDCC. A VME accessible register at address Base+$62 allows to make the selection:

Data	Clock
0	Internal 40 MHz
1	Internal 10 MHz
2	External ECL
3	External NIM

The selected clock is then applied to 2 4 bit programmable delay lines (PECLDL-2.8-2.0) and distributed (10E116) and translated to TTL (10ELT25) to give the internal clocks $BC0_n$ and $BC1_n$. The delays of BC0 and BC1 are set according to the content of the VME accessible register at address Base+$60 as following:

Data	Delay
D3..D0	Delay BC0 = value * 2 ns (minimum 2.8 ns)
D7..D4	Delay BC1 = value * 2 ns (minimum 2.8 ns)

1.3.3.3. Temperature measurement.

Two temperature captors (TMP36FT9 from Analog Devices) allow to control the temperature of the module with a 0.5 LSB/ºC sensitivity and 38 LSB representing 25ºC. The temperature measurement is accessible at the VME address Base+$63 after the conversion has been requested by a write access at the same address with the following value:

Data	Selected captor
$A5	Captor 1
$A6	Captor 2

Important remarks:

1. The read value is valid only after the second conversion.
2. The conversion duration is 4,5 µs. During that time no VME Dtack is given.

1.3.3.4. Power voltages measurement.

The CTPD is powered either directly from the VME backplane or through voltage regulators. The following voltages are required:
+ 5V, + 3.3V, - 2V, - 4.5V, - 5.2V.
All of them except - 4.5V can be measured by an ADC (MAX155). The voltage measurement is available at the VME address Base+$63 after a conversion has been requested by a write access at the same address:

Data	Selected Voltage	Sensitivity	Nominal Value
$A2	+ 5V	12.8 Lsb/V	64 Lsb
$A7	+ 3.3V	25.6 Lsb/V	84.5 Lsb
$A4	- 2V	51.2 Lsb/V	154 Lsb
$A3	- 5.2V	12.8 Lsb/V	180 Lsb

Important remarks:

1. The read value is valid only after the second conversion.
2. The conversion duration is 4,5 µs. During that time no VME Dtack is given.

1.3.4. TSTPAT block.

This block provides 32 bit test patterns TST<31..0> at the input of the VLP block. These patterns are synchronous with respect to the internal clock BC0. There are coming from either a large memory block or from a pseudo-random generator. A CPLD (EPM7128EQC160-10P from Altera) named TSTG in the drawing, controls this block. The principle scheme is given in figure 4.

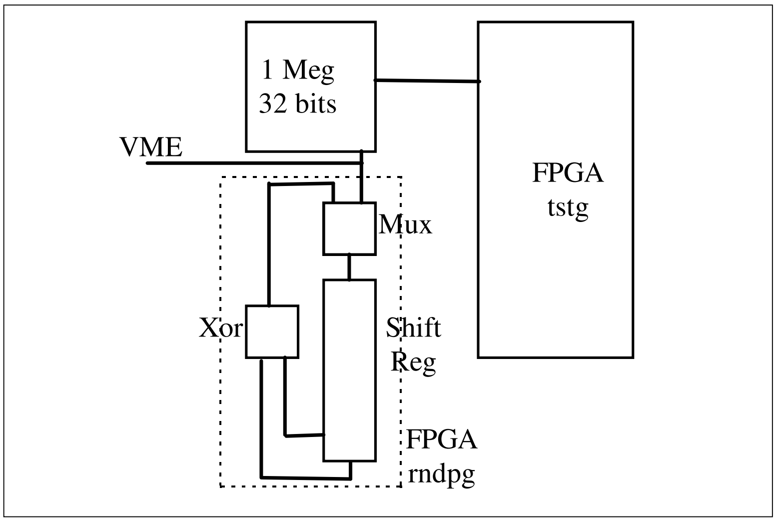


Fig. 4. Test pattern generation

1.3.4.1. The memory block.

This memory has a size of 1 mega 32 bit words (8*KM64BV4002) allowing a test period of 26.2 ms. It is accessible through the VME interface. The access are controlled by a CPLD referenced TSTPG. It also contains the address counter which can be accessible through VME and which is automatically incremented during the test.

1.3.4.2. The pseudo-random generator (PRBS)

It consists of a shift register with feedback. The register length is 31 bit and the pseudo-random sequence is obtained by x-oring the positions 31 and 28. The sequence duration is 53 s.
A FPGA (EPF 81500ARC240-2) referenced RNDPG contains the 32 registers and the associated logic.
Remark:

- This method allows to have 0 or 1 with the same probability for each test bit. The sequence depends on the initial values in the shift registers. These initial values are the first locations of the memory.

- If one starts with all shift register bits set to 0, the output will always be 0.

1.3.4.3. VME access to the TSTPAT block.

The memory is accessible through VME at the address $200000 to $2FFFFE when not used as pattern generator.
A VME register at address $100 controls the test pattern generation. If bit 0 of this register is set to 1, the memory generates test patterns. If the bit 1 is set, the pseudo-random generator is used.
Set the bits 0 or 1 of this register has the following effects:

- Clear the VLP block registers contents.
- Release the clear of the pseudo-random generator registers.
- Initialise to 0 the memory address counter.
- Enable the memory address counter.
- Enable the test inputs of the VLP block.

1.3.5. The LMV block.

This block contains the look-up table and the associated logic of mask and veto which will form the level-1 decision.

1.3.5.1. The look-up table.

Its scheme is given in figure 5.

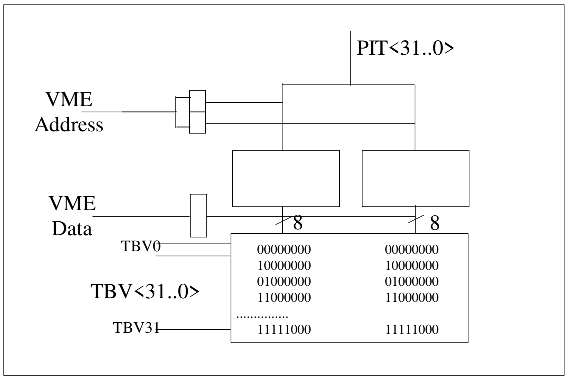


Fig. 5. Look-up Table

The look-up table allows to form 32 trigger candidates out of the 2^{32} possible combinations. It is done with 2 fast static RAMs (MCM6726BWJ10) referenced RAM015, associated with an arbitrary combinatorial logic included in 2 CPLD (EPM7128EQC160-10P) referenced VAM1631. The combinatorial logic is indicated in the figure 5. The memory can be read and write through VME.

1.3.5.2. Mask and veto.

The principle is given in figure 6.

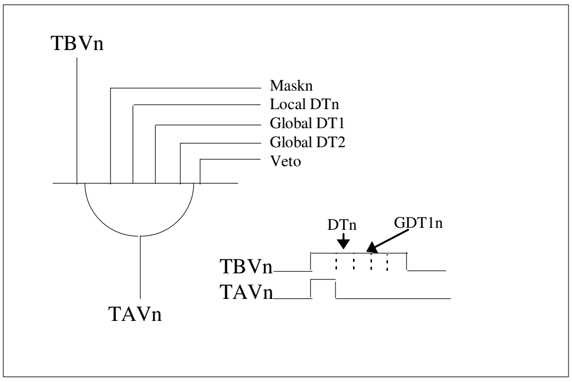


Fig. 6. Mask and Veto principle

We get one of the 32 trigger candidates in making an AND of the look-up table output (TBVn) and the following signals:

- Maskn: individual mask set in a VME register.
- Veto: global external Veto signal.
- Global DT1: signal given by the RDOUT block which introduces a programmable duration dead-time after each L1A.
- Global DT2: signal given by the CODT block which introduces dead-time so that the total number of L1A in a given time does not exceed a programmable value (eg. No more than 16 L1A within 16 μs).
- Local DTn: individual dead-time signal coming from the prescalers.

This AND is included in the CPLD's VAM105 and VAM1631.

1.3.5.3. VME commands.

The look-up table memory is accessible (read and write) in 16 bit mode at the VME addresses $090000 to $09FFFF.
The VME access to the memory puts the PIT<31..0> in high impedance.
The mask register is accessible at the VME address $120.

1.3.5.4. Performances.

The simulation of the LMV block gives the following results:

- PITn to TAVm : 20 ns nominal.
- PITn to TBVm: 20 ns nominal.

1.3.6. The PRES block.

This block allows to reduce the frequency of the trigger candidates. It contains 32 rate dividers with a programmable divider coefficient from 1 to 4096. It is done with 2 FPGA's (EPF81500ARC240-2) referenced HEXCALUX. They are clocked with BC1.

1.3.6.1. VME commands

The registers which give the divider coefficients are accessible (Read and Write) in D32 at the VME addresses $160 to $17E.
The prescalers contents are accessible (Read only) in D32 at the VME addresses $140 to $15E.
The data format is the following:

D<31..28>	D<27..D16>	D<15..12>	D<11..0>
xxxx	TAV<n+16>	xxxx	TAV<n>

Remarks:

- The outputs TAP<31..0> are active when the precount is reached.
- The actual division factor is equal to 1 + the content of the register.

1.3.6.2. Performances.

The simulation of this block gives the following results:

- Set-up time TAV to BC1: 0 ns.
- Propagation delay BC1 to TAP: 12.1 ns.

1.3.7. The CNTS block.

The 3*32 counters of this block allow for real time monitoring of various internal trigger patterns rates: PIT, TBV and TAP. These 12 bit counters can accommodate any rate within one LHC turn. The bunch counter reset (BCR) or a VME key address access load the content of these counters to an associated read-out register and reset the counters. The read-out can then be done during the following LHC turn.
Three FPGA's (EPF81500ARC240-2) referenced FASCAL are used to implement this functionality. The principle is given in figure 7.

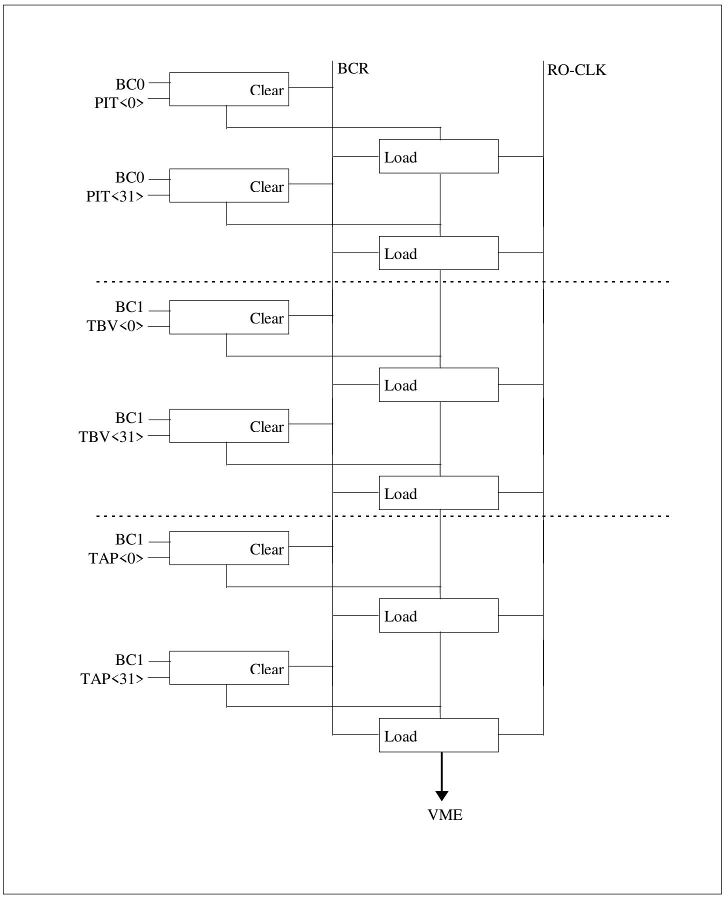


Fig. 7. Monitoring scalers.

1.3.7.1. VME commands.

The read-out registers are read-out sequentially in D16 at the VME address $180. The read-out order is the following:

- TAP<31> 1st word
- ...
- TAP<0> 32nd word
- TBV<31> 33rd word
- ...
- TBV<0> 64th word
- PIT<31> 65th word
- ...
- PIT<0> 96th word

The counters are loaded in the read-out registers on receipt of BCR or after a VME write access at the address $180.

1.3.7.2. Performances.

The simulation gives the following results:

- Set-up time TAP, TBV, PIT to BCn: <3.3 ns.
- Working frequency: 55 MHz.

1.3.8. The RDOUT block

This block contains the necessary resources to:

- Form the final L1A signal before its transmission to the IOCON block.
- Form the bunch crossing number (BCID) and reset it on receipt of BCR.
- Form the L1A number (L1ID).
- Align the various internal trigger patterns (PIT, TAV, TAP, BCID) to the same bunch crossing.
- Generate the dead-time associated with each L1A.
- Measure the dead-time duration.
- Load in Fifo's the internal trigger pattern (PIT, TAV, TAP) and the identifiers (BCID, L1ID) and keep these information until the read-out is done.

1.3.8.1. L1A signal generation.

This signal is the OR of PIT<31..0> gated by an Enable signal. This Enable allows to isolate the CTPD from the modules placed after it in the trigger chain. This function is done in a fast CPLD (EPM7032LC44-6) and the principle is given in figure 8.

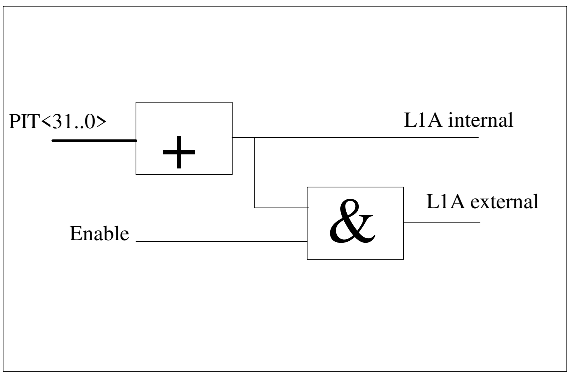


Fig. 8. L1A generation.

The Enable signal is activated when a "1" is written in position 7 of the register accessible at VME address $80.

1.3.8.2. BCID generation.

The BCID counter is a 12 bit counter which is incremented at each BC1 and reset when it receives BCR.

1.3.8.3. L1ID generation.

The L1ID counter is a 16 bit counter which is incremented when L1A is issued. It is reset when a "1" is written at position 2 of the VME register accessible at address $80.

1.3.8.4. Alignment of the bit patterns and the BCID.

Before being written in the read-out Fifo's, the bit patterns and the BCID have to be aligned to take into account the latency of the different elements. This alignment is done by inserting some shift register positions for each of these bits. These shift registers are implemented by mean of a shift of the write and read Fifo's pointers. These synchronous Fifo's (8 k words of 18 bits, IDT72255-15) can accommodate a minimal 14 step shift between the read and the write pointers. The initialisation and the shift value is done by writing a "1" in position 0 of the register accessible at the VME address $80. The FPGA referenced ROCD handles these operations.

The implementation of the shift registers is the following:

1. Shift register associated to PIT<31..0>:
- Write clock: BC0.
- Read clock: BC1.
- Shift value between read and write VME address $81.
2. Shift register associated to TAV<31..0>:
- Write clock: BC1.
- Read clock: BC1.
- Shift value between read and write VME address $82.
3. Shift register associated to TAP<31..0>:
- Write clock: BC1.
- Read clock: BC1.
- Shift value between read and write VME address $83.
4. Shift register associated to BCID:
- Write clock: BC1.
- Read clock: BC1.
- Shift value between read and write VME address $84.

Remark concerning the registers which contain the shift value:
The actual shift value is 14 if the content of the register is less or equal to 14.

1.3.8.5. GDT1 dead-time generation.

The GTD1 dead-time signal is the OR of:

- A programmable dead-time duration associated with each L1A. The duration in number of BC is in the register accessible at VME address $89. The actual duration is the register content + 1.
- A dead-time signal introduced when the read-out Fifo's are almost full (128 remaining positions in the Fifo's). This signal is enable the position 6 of the VME register accessible at address $80 is "1".

- A permanent dead-time if the position 5 of the VME register accessible at address $80 is “1”.

1.3.8.6. Dead-time duration measurement.
A 32 bit counter is incremented at each BC1 during the global dead-time duration (including Veto, GTD1 and GTD2). This counter is reset by writing “1” in position 4 of the VME register accessible at address $80.
The counter content is accessible (read) at the VME address $A0.

1.3.8.7. VME read-out Fifo’s.
Each time a L1A is generated and during a programmable window (nominal width +- 3 BC), the bit patterns PIT, TAV, TAP and the content of BCID and L1ID counters are written in Fifo. This 8 k word Fifo (8 IDT72255-15) allows to store about 2 s of data for a 400 Hz L1A rate.
The time window to be read-out is stored in the VME register accessible at address $86 (actual width = content + 1 BC).
The start position of the window with respect to L1A is defined by 4 bits in the VME register accessible at address $85.
The VME access to the Fifo’s can be done in block mode (AM code $0B or $0F) or in single word access, at the VME address $C0.
The data format is the following:

	D<31..16>	**D<15..0>**	
Word n	PIT<31..16>	PIT<15..0>	BCn
Word n+1	TAV<31..16>	TAV<15..0>	BCn
Word n+2	TAP<31..16>	TAP<15..0>	BCn
Word n+3	BCID	L1ID	BCn
Word n+4	PIT<31..16>	PIT<15..0>	BCn+1
Word n+5	TAV<31..16>	TAV<15..0>	BCn+1
Word n+6	TAP<31..16>	TAP<15..0>	BCn+1
...	...	...	...

When the Fifo’s are empty a VME BERR is generated in answer to a read access.
The status flags of the Fifo’s are accessible at the VME address $87 for the “empty” flags and $88 for the “almost full” flags.

The control logic of the Fifo's, the counters and registers are implemented in a FPGA (EPF81500ARC240-2) referenced ROCD.

1.3.9. The CODT block.

The block generates the GDT2 signal which is sued in the LMV block. This signal contributes to the overall dead-time in limiting the number of L1A during a given time (for instance no more than 16 L1A in any 16 µs).
The implementation principle is given in figure 9.

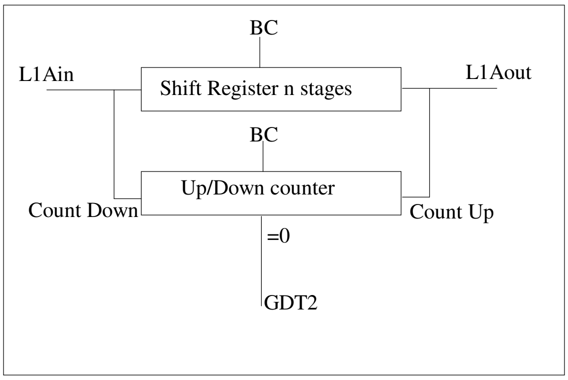


Fig. 9. GDT2 dead time generation.

The L1A signal are stored in a shift register clocked by BC1. They exit this register n * 25 ns latter. An up/down counter, with an initial value of m, is decremented when a L1A enters the shift register and is incremented when a L1A exits the shift register. If the counter reaches "0", it means that there are m L1A within n*25 ns and that a dead-time must be introduced.
The shift register is made with a Fifo (IDT72255-15). The register length is programmable by mean of a VME register accessible at the address $E2. The length is:

- if data <14 length = 8 * 14.
- if data >13 length = 8 * (data+1).

The initialisation and the pointers shift is done by writing "1" in position 1 of the VME register accessible at address $E0.
The Up/Down counter and the associated logic are implemented in one CPLD (EPM7128EQC160-10P) referenced CADT. This counter is loaded by writing the 6 low order bits of the VME register accessible at address $E1. Its value is in the range 0..63.
The GDT2 signal is enabled if the position 0 of the VME register accessible at address $E0 is "1".

1.3.10. The PLDCFG block.

This block contains the necessary resources to configure the "in-circuit configuration" of the 8 "SRAM-based" FPGA's (VLPL, RNDPG, 2 * HEXCALUX, 3 * FASCAL, ROCD). These devices are configured together in a parallel fashion. The configuration data are written through the VME in a memory (256k*16 bit, TC514161FFL-70L). These data are generated in combining the SOF files provided by the ALTERA Maxplus compiler (See ALTERA application note 38). The content of the memory is then transfered in parallel to all the FPGA (one bit per FPGA) under the control of a CPLD (EPM7128EQC160-10P) referenced CFGC. Each FPGA receives its 250000 configuration bits with a 2 MHz clock (derived from the VME Sysclock) and the proper configuration and status bits.

1.3.10.1. VME commands.

The memory which contains the configuration data is accessible through VME in D16 mode at the address $40000 to $7ffff.
The FPGA configuration starts when a write access at the position 0 of the VME register accessible at address $20 occurs. Writing a "0" resets the devices. A "0" to "1" transition starts the configuration process.
During the configuration, the status of the FPGA's can be read-out at the VME address $21 to check the operation is well going on. If an error occurs, the status bit remains low. The state of the state machine which controls this operation can be read at the address $20.

1.3.11. The PLDJTG block.

This block gives the necessary signals to control the JTAG chain which links the CPLD's and the FPGA's of the module. This JTAG chain consists of the following:

- A TDI/TDO daisy chain which links the components in the following order: CFGC, ROCD, FASCAL, HEXCALUX, HEXCALUX, CADT, VAM015, VAM1631, FASCAL, FASCAL, RNDPG, TDCC, VLPL, TSTG. Each component can be isolated by means of a dual invertor made with a 2*3 pins socket and 2 jumpers.
- The individual TMS lines.
- The individual RST lines.
- A common TCK clock line.

This JTAG chain could be used for the following:

- Test of the interconexions.
- Programmation of the next generation of CPLD EPM7128S. This would avoid the use of expensive and potentially unreliable sockets for these circuits.

The PLDJTG block is made with a CPLD (EPM7128EQC160-10P) referenced JTGC. This CPLD is now installed on a socket and it will be possible in the future to use an EPM7128S. A Bitblaster port will allow an in-situ modification.

1.3.11.1. VME commands.

Two VME registers are accessible (Read and Write): TMSreg at the address $41 and RSTreg at the address $40. The bit 0 of TMSreg is the input of the JTAG daisy chain (TDI). Each write access in TMSreg leads to a JTAG clock period generation (TCK). The end of the daisy chain (TDO) is in the bit 0 of the VME register accessible at address $42.

1.3.12. The VMEINTER block.

This block contains the VME slave interface of the CTPD. In addition to the data and address drivers and receivers, two hexadecimal rotary switches allow to set the base address. The address decoding is done in a CPLD (EPM7128EQC160-10P) referenced VMED. This CPLD is now installed on a socket and it will be possible in the future to use an EPM7128S. A Bitblaster port will allow an in-situ modification.

1.4. Timing.

The figure 10 gives all the timing information concerning the described blocks. The timing diagram is given in figure 11.

The following main parameters can be extracted:

- The minimum delay between the input bits XSDP and the L1A output is 60.5 ns.
- There three loops with critical timings:

1. BC1, TAP, TAV, BC1 22/25 ns.
2. BC1, GDT1, TAV, BC1 22/25 ns.
3. BC1, GDT2, TAV, BC1 20/25 ns.

The figure 12 shows the relationship between the different timing signals (XSDC, BC0, BC1) and their phase difference.

These figures show that:

- The phase difference which is measured is:
  $(t_{xsdcn} + 1\ ns) - (t_{bc0} - 3.5\ ns)$
- The position of BC0 with respect to XSDP is:
  $t_{xsdp} - t_{bc0} > -3ns$

In other words, if XSDC and XSDP are in phase, the measure of the difference is 1.5 ns.

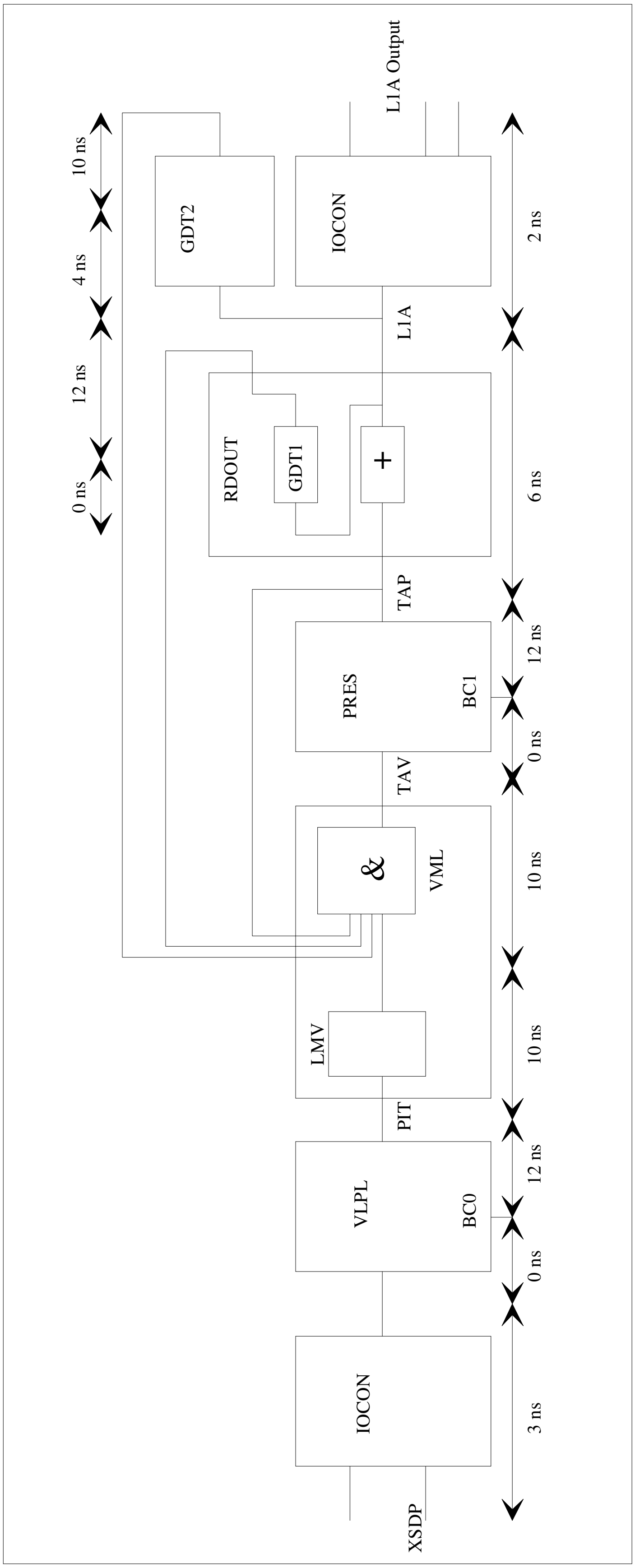


Fig. 10. CTPD timing (main flow).

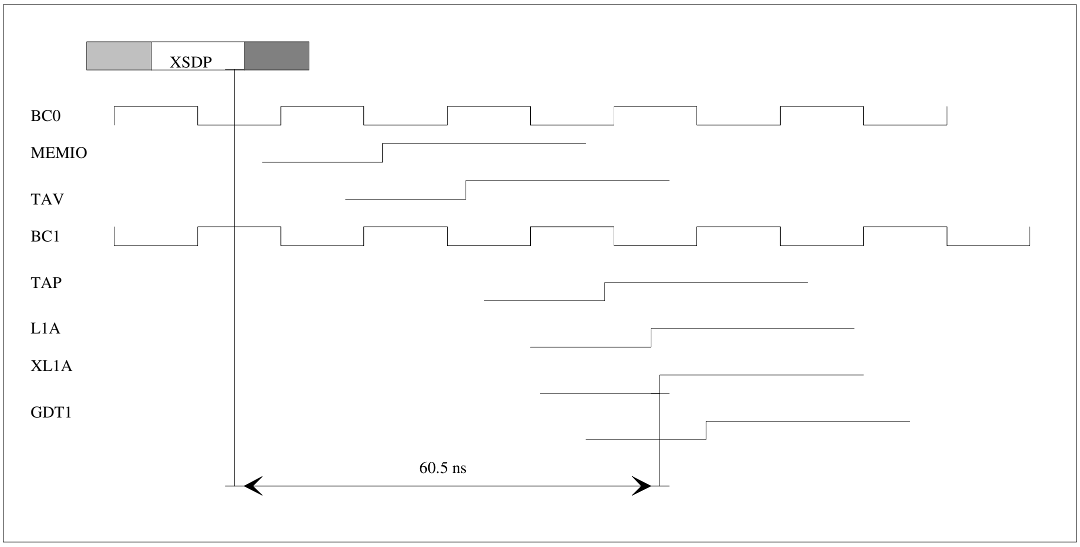


Fig. 11. CTPD timing diagram.

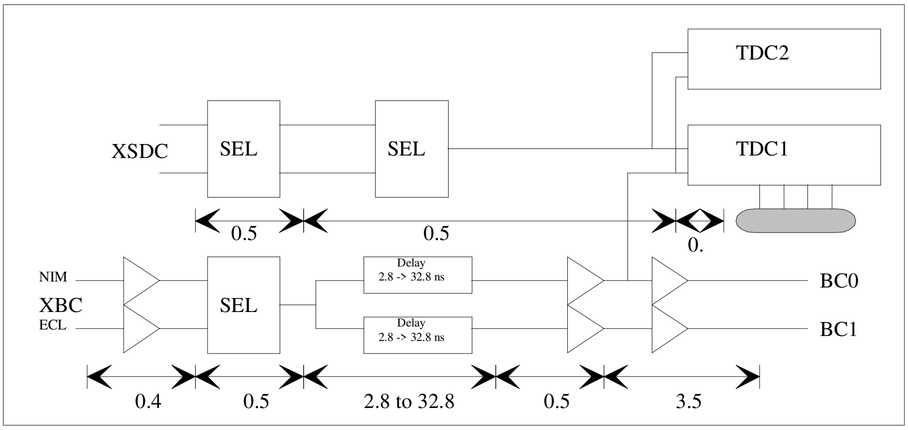


Fig. 12. Clock generation and phase measurement.

2. User's Guide.

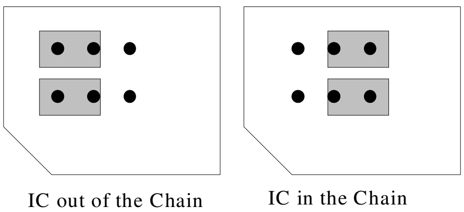
Important warnings:

1. The crate must be powered down before the CTPD is inserted.
2. Some components of the CTPD are sensitive to static discharges. To avoid damages, minimise handling and take appropriate precautions against static discharges.
3. The large scale integrated circuits with QFP packages should only be replaced by a specialist in a laboratory environment (pins tend to bend, causing short circuits).
4. The CTPD must be secured with the top and bottom fixing screws.
5. Stupid people are even not allowed to look at this module.

2.1. Installation procedure.

The VME base address is set before use by the means of the 2 hexa-decimal switchs SW1 and SW2 as shown in figure 13. SW2 is used to define addresses <31..28> and SW1 for <27..24>.

The JTAG daisy chain must be set in inserting 2 jumpers at the level of each chip which has to be inserted in the chain. The jumper position is as follows:



The connectors are associated to the chips as follows:

Connector #	IC type	Reference	Page
J6	EPF81500ARC240-2	Hexcalux	PSH
J7	EPF81500ARC240-2	Fascal	SCA3
J8	EPF81500ARC240-2	Rocd	RDCTRL
J9	EPM7128EQC160-10P	Chgc	CFGCTR
J10	EPM7128EQC160-10P	Tstg	GECTAL
J11	EPF81500ARC240-2	Vlpl	VLPL
J12	EPM7128EQC160-10P	Tdcc	TDCCTRL
J14	EPF81500ARC240-2	Rndpg	RNDGE
J15	EPF81500ARC240-2	Fascal	SCA2
J16	EPF81500ARC240-2	Hexcalux	PSL
J17	EPF81500ARC240-2	Codt	CODT
J18	EPM7128EQC160-10P	Vam015	VML
J19	EPM7128EQC160-10P	Vam1631	VMH
J20	EPF81500ARC240-2	Fascal	SCA1

Remark:

- The CPLD's EPM7128E... do not include JTAG. These circuits can be replaced by the EPM7128S type which includes JTAG and can be configured through this channel.

2.2. Front Panel.

The front panel is shown in figure 14 as well as the lay-out of the connectors.

Output L1A:

- NIM coaxial Lemo 00.
- Differential ECL 2 * 100 Ω @-2V.

Input SDP+SDC:

- Differential ECL 2 * 50 Ω @-2V.
- Connector 100 pins type P50E100P1SR1.

Input Veto:

- NIM coaxial Lemo 00. 50 Ω @0V.

Input BCR:

- NIM coaxial Lemo 00. 50 Ω @0V.

Input BC:

- NIM coaxial Lemo 00. 50 Ω @0V.

- Differential ECL 2 * 50 Ω @-2V.

The unused inputs can be left open.

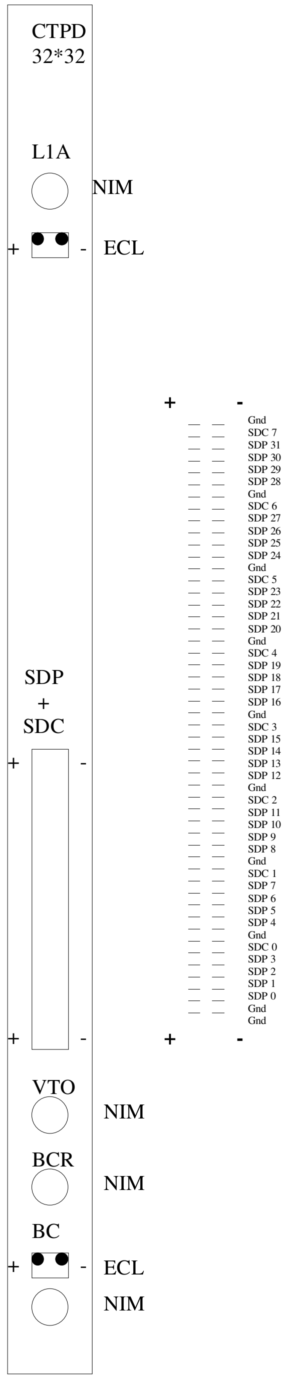


Fig. 14. CTPD front panel.

2.3. Programming the CTPD.

2.3.1. VME mapping summary.

The following tables give the VME mapping of the CTPD.

Name	Address	Size	Bit	Access	Sysreset	Meaning
PLDCFG	$20	Word				
			0	R/W	x	0: reset FPGA for configuration 0 to 1: start configuration
			1	R	x	0 until configuration is finished
			2	R	0	Internal state machine
			3	R	0	Internal state machine
			4	R	0	Internal state machine
			5..15	R	0	Unused
PLDCFG	$21	Word				
			0	R	x	VLPL FPGA status. 0 during 100 ms after power up. Held low if configuration error.
			1	R	x	Idem for RNDPG
			2	R	x	Idem for HEXCALUX (PSL)
			3	R	x	Idem for HEXCALUX (PSH)
			4	R	x	Idem for FASCAL (SCA1)
			5	R	x	Idem for FASCAL (SCA2)
			6	R	x	Idem for FASCAL (SCA3)
			7	R	x	Idem for ROCD
PLDJTG	$40	Word				
			0	R/W	0	Reset or initialise the boundary scan of VLPL. Should be low during user-mode operation.
			1	R/W	0	Idem for RNDPG
			2	R/W	0	Idem for HEXCALUX (PSL)
			3	R/W	0	Idem for HEXCALUX (PSH)
			4	R/W	0	Idem for FASCAL (SCA1)
			5	R/W	0	Idem for FASCAL (SCA2)
			6	R/W	0	Idem for FASCAL (SCA3)
			7	R/W	0	Idem for ROCD
			8..15	R	0	Reserved

PLDJTG	$41	Word				
			x	W	x	Each write at this address generates a JTAG clock (TCLK)
			0	R/W	0	Start of chain TDI signal
			1	R/W	0	Reserved
			2	R/W	1	Select the JTAG mode for VLPL (TMS). Should be 1 in user-mode operation.
			3	R/W	1	Idem for RNDPG
			4	R/W	1	Idem for TSTG
			5	R/W	1	Idem for VAM015
			6	R/W	1	Idem for VAM1631
			7	R/W	1	Idem for HEXCALUX (PSL)
			8	R/W	1	Idem for HEXCALUX (PSH)
			9	R/W	1	Idem for FASCAL (SCA1)
			10	R/W	1	Idem for FASCAL (SCA2)
			11	R/W	1	Idem for FASCAL (SCA3)
			12	R/W	1	Idem for ROCD
			13	R/W	1	Idem for CADT
			14	R/W	1	Idem for CFGC
			15	R/W	1	Idem for TDCC
PLDJTG	$42	Word				
			0	R	x	Output of the JTAG chain (TDO) If all chips are in the chain, the order is TDI → cfgc, rocd, fascal (SCA3), hexcalux (PSH), hexcalux (PSL), cadt,vam015, vam1631, fascal (SCA2), fascal (SCA1), rndpg, tdcc, vlpl, tstg → TDO
			1..15	R	0	Reserved
TDC	$60	Word				
			0..3	R/W	x	BC0 delay. 2ns / LSB from 2.8 to 32.8 ns.
			4..7	R/W	x	Idem for BC1.
TDC	$61	Word				
			0..5	R/W	x	Selection the signal to measure: 5 4 3 2 1 0 1 0 x x 0 0 SDC0 1 0 x x 0 1 SDC1 1 0 x x 1 0 SDC2 1 0 x x 1 1 SDC3 1 1 0 0 x x SDC4 1 1 0 1 x x SDC5 1 1 1 0 x x SDC6 1 1 1 1 x x SDC7 0 0 x x x x BCR 0 1 x x x x Veto
			6..7	R/W	x	Reserved

TDC	$62	Word				
			0..1	R/W	x	Clock selection: $2 Ext ECL $3 Ext NIM $0 Internal 40 MHz $1 Internal 10 MHz
			2..5			Unused
			6..7	R		Reserved
TDC	$63	Word				
			0..7	W	x	Selection of measurement: $A2 +5V $A7 +3.3V $A4 -2V $A3 -5.2V $A5 Temperature capture 1 $A6 Temperature capture 2 $E0 Phase difference between BC0 and the signal selected in TDC $61
			0..7	R	x	Measurement result. After a change of selection, the result is valid on the second read only. A measurement takes about 4.5 µs.
TDC	$64	Word	0..7	R	x	Phase measurement of the selected signal with respect to BC0. Value is between 0 and 9.
RDOUT	$80	Word				
			0	W	x	Ored with Sysreset. When a 1 is written, the alignment Fifo’s are initialised.
			1	W	x	Ored with Sysreset. When a 1 is written, the read-out Fifo’s are initialised.
			2	W	x	Whe a 1 is written, the L1A counter is reset.
			3	W	x	Ored with Sysreset. When a 1 is written, the read-out Fifo’s selector is initialised.
			4	W	x	Ored with Sysreset. When a 1 is written, the dead-time counter is reset.
			5	R/W	0	When equal to 1, a permanent GTD1 dead-time is generated.
			6	R/W	0	When equal to 1, the “almost full” flag of the read-out Fifo’s introduces dead-time.
			7	R/W	0	When equal to 1, the L1A generation is enable.
RDOUT	$81	Word				
			0..7	R/W	x	Define the number of steps for the alignment of PIT<31..0>. The actual number number of steps is 1 + the register value with a minimal value of 14.
RDOUT	$82	Word				
			0..7	R/W	x	Idem for TAV<31..0>.

RDOUT	$83	Word	0..7	R/W	x	Idem for TAP<31..0>.
RDOUT	$84	Word	0..7	R/W	x	Idem for BCID<11..0>.
RDOUT	$85	Word	0..3	R/W	x	Define the beginning of the read-out window.
RDOUT	$86	Word	0..7	R/W	x	Define the width of the read-out window. The actual width is 1 + the register value.
RDOUT	$87	Word	0..7	R	x	Empty flag status of the read-out Fifo’s. 0 means Fifo empty. 0 PIT<15..0> 1 PIT<31..16> 2 TAV<15..0> 3 TAV<31..16> 4 TAP<15..0> 5 TAP<31..16> 6 BCID<11..0> 7 L1ID<15..0>
RDOUT	$88	Word	0..7	R	x	Almost full flag status of the read-out Fifo’s. 0 means Fifo almost full. 0 PIT<15..0> 1 PIT<31..16> 2 TAV<15..0> 3 TAV<31..16> 4 TAP<15..0> 5 TAP<31..16> 6 BCID<11..0> 7 L1ID<15..0>
RDOUT	$89	Word	0..7	R/W	x	Define the dead-time in number of BC introduced after each L1A. The actual value is 1 + the register value.
RDOUT	$A0	Long	0..31	R	0	Dead-time counter.
RDOUT	$C0	Long	0..31	R	0	Access to the read-out Fifo’s. Either single access or block mode access. If the Fifo’s are empty a BERR is issued. The data format is: PIT of BCn TAV of BCn TAP of BCn BCID and L1ID PIT of BCn+1 ...

CODT	$E0	Word				
			0	R/W	x	When equal to 1 it enables the GDT2 dead-time signal.
			1	W	x	Ored with Sysreset. Writing a 1 initialises the Fifo's used as delay line.
CODT	$E1	Word				
			0..5	R/W	0	Define the maximum number of L1A is the window duration defined in CODT $E2.
			7	R	0	Equal to 1 during the GDT2 dead-time duration.
CODT	$E2	Word				
			0..7	R/W	x	Define the window duration during which the number of L1A is limited. The actual duration is 8 * (data + 1) with a minimum of 8 * 14 number of BC.
TSTPAT	$100	Word				
			0	R/W	0	The memory gives test pattern when this bit is 1.
			1	R/W	0	The pseudo random generator gives test pattern.
			2..7	R/W	0	Reserved.
LMV	$120	Long				
			0..31	R/W	x	Masks of each L1A candidates.
PRES	$140 to $15E	Long				
			0..11	R	x	Prescalers 0 to 15.
			16..27	R	x	Prescalers 16 to 31.
PRES	$160 to $17E	Long				
			0..11	R/W	x	Division rate factor of the prescalers 0 to 15.
			16..27	R/W	x	Division rate factor of the prescalers 16 to 31. The actual division rate factor is 1 + the register content.
CNTS	$180	Word				
			11..0	R	x	VME read access to this address leads to the transfer of the 96 scalers to the VME. The read-out order is: TAP<31> ... TAP<0> TBV<31> ... TBV<0> PIT<31> ... PIT<0>
			x	W	x	Ored with BCR. Writing 1 transfers the scalers content to the read-out

						register and resets the scalers.
PLDCFG	$40000	Word	x	R/W	x	Memory which contains the configuration bits of the FPGA. Bit 0 is for VLPL Bit 1 is for RNDPG Bit 2 is for HEXCALUX (PSL) Bit 3 is for HEXCALUX (PSH) Bit 4 is for FASCAL (SCA1) Bit 5 is for FASCAL (SCA2) Bit 6 is for FASCAL (SCA3) Bit 7 is for ROCD
LMV	$90000	Word	0..15	R/W	x	Base address of the 64 k words look-up memory.
TSTPAT	$200000	Long	0..31	R/W	x	Base address of the 1 Mega long words memory which contains the test pattern.

2.3.2. FPGAs and CPLDs (re)configuration.

After the module has been powered up, the FPGA's and CPLD's have to be configured. This operation is defined by Altera and it is mandatory to read the application notes AN33 and AN38 from Altera.

2.3.2.1. FPGAs (re)configuration.

A source file in AHDL (xxx.tdf) is associated with each FPGA. This source file has to be compiled by the MaxPlus2 compilator with the parameter file MD-PSB (multiple device passive serial bit-slice). The object files (xxx.sof) have then to be combined in the proper order in a single TFF file. The first xxx.sof file correspond to the LSB of the TFF file. This TFF file has then to be converted from ASCII to binary before being written in the CPLD configuration memory (PLDCFG $40000).

The configuration process can then be started by writing 1 in the bit 0 of the PLDCFG $20 register. The duration of this process is about 100 ms and the read-out of the bit 1 of the above register indicates if the operation was or not successful.

There is no automatic reconfiguration. The register PLDCFG $21 has to checked. A transition 1 to 0 in this register indicates an error either during the configuration process or during the normal running (eg. Power down,...). If this happens, the full configuration process has to be restarted in writing 0 in the bit 0 of PLDCFG $20 and then in writting 1 at the same location.

2.3.2.2. CPLDs (re)configuration.

Two types of CPLD, pins to pins compatible can be installed in the CTPD. They are EPM7128EQC160-10P and EPM7128SQC160-10P. The "S" version will be soon available and will allow an in-situ programmation with the JTAG chain.

The necessary resources to support these chips exist in the CTPD. Only the 2 CPLD's referenced JTGC and VMED have to be always programmed with a bit-blaster.

2.3.3. Operating the module.

When the configurable chips and the JTAG chain are in user mode, the module has to be initialised with the following sequence of instructions:

1. Clock selection. ($62)
2. Phase alignment of BC0 and BC1 (nominal value 12 ns). ($60)
3. Disable the L1A output. ($80)
4. Enable the dead-time GDT1. ($80)
5. Disable the dead-time GDT2. ($E0)
6. Mask the trigger generation. ($120)
7. Write the look-up table. ($90000)
8. Write the prescale factors. ($160 to $17E)
9. Align the different bit patterns. ($81 to $84)
10. Initialise the Fifo's. ($80)
11. Define the read-out window position. ($85)
12. Define the read-out widow width ($86)
13. Define the dead-time duration to be introduced after each L1A ($89). Note that one should not have more than one L1A within the read-out window width.
14. Define if necessary the dead-time GDT2. ($E0 to $E2)
15. Reset all the counters. ($80 and $180)
16. Enable the CTPD:

- GDT1 permanent dead-time suppression.
- GDT2 activation.
- Remove masks.
- Enable L1A.

The module is now ready to receive test patterns or external inputs.

The alignment operations concerning the external inputs are done in the FPGA VLPL. Any modification requires a recompilation of the .tdf file and a reconfiguration of the FPGA.

2.4. Tests.

The functional test of the module is done with the internal test pattern generators. The description of these test generators is in 1.3.4.

3. Hardware Manual.

3.1. Introduction.

The top-down method has been used to design this module. From the specifications, a block diagram has be made. Then each block has been described and synthesised into CPLDs and FPGAs. A functional simulation of each block has been done and then a simulation of the full module has been performed. CADENCE CAE tools have been used as well as the Altera tools. The PCB lay-out has been done with the Allegro router from CADENCE.

3.2. Circuit diagrams.

The circuit diagrams are given in annex A and are presented hierarchically.

3.3. FPGAs and CPLDs source files.

The text file xxx.tdf containing the source equations in AHDL are given in annex B.

3.4. Simulation.

A detail of the simulation results, including the stimuli files is given in annex C.

3.5. PCB

The annex D gives the specifications of the PCB as well as a view of the different layers. The strip and microstrip lines have a characteristic impedance of approximatly 55 Ω. Termination resistors have been included for long lines.

3.6. Parts list.

The parts list is given in annex E.

3.7. Hardware tests.

The JTAG chain allows a boundary scan test of a part of the circuit. The expected behaviour as well as the interconnexions which can be tested are given in annex F.