DRAFT
Programming the Front End Module

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March 21, 1997

1 Introduction

(to be filled)

2 The Board

(this section is still incomplete)

2.1 VMEbus interface

The FEM is accessible by VME bus either in 16 bit or in 32 bit data mode. The lowest 16 bit of the 24 bit address are used by the FEM. This means that there are 64 kByte address space. The lowest 32 kByte are occupied by the dual ported RAM. The upper half is used for programming and resetting the xilinx. The VMEbus interrupt capability is also configured at this place. The memory map of the FEM is shown in figure 1.

The upper 8 address bits of the 24 bit FEM address are defined by switches on the board. So the base address of the board can be configured in steps of 64 kByte. In the following all addresses are given relative to this base address.

2.2 Front panel LEDs

Eight LEDs are controlled by the FEC. Table 1 lists their meanings. LED on represents an active status of the corresponding signal.

3 The FrontEndController

The FrontEndController (FEC) is responsible for the communication between the FeAsics and the VME-Bus. Its tasks are:

- Configuration of FeAsics
- Fast readout of FeAsics

(to be filled)

Figure 1: Memory map of the Front End Module

LED	Description
1	Light
2	InputMode
3	ReadoutActive
4	EnableStatusWrite
5	EqualReadout1
6	EqualReadout2
7	SpyBusMode
8	SerialRdy

Table 1: LEDs on the front panel controlled by the FEC

- Generation of additional Level1Accept-Signals for test purposes
- Readout of the SpyBus of FeAsics

The FEC is implemented on a Xilinx FPGA of the type XC4010E-3. The FPGA is directly configured over the VME-Bus. A dual ported RAM is integrated on the FEM for buffering data. Its size is 32 kBytes.

3.1 Configuring the FPGA

The FPGA is configured directly over the VME-Bus in asynchronous peripheral mode. The configuration data is written bytewise to the byte-address 0xC003 relative to the base address of the FEM. Since the FPGA needs some time to internally serialize the data, it is necessary to test if it is ready to accept the next byte. This is done by reading the byte-address 0xC003. Bit 7 gives the status of the FPGA, 1 means ready, 0 busy.

The startup-sequence of the FPGA is controlled by the Configuration Clock, which is only generated, when data is written to the FPGA. It is important to supply enough data for completion of the startup-sequence.

To reprogram the FPGA a negative pulse can be given to the PROGRAM pin of the FPGA. Then the configuration memory is cleared and the FPGA waits for new configuration data. To give this reprogramming pulse write to the byte-address 0xE003 with the lowest bit set. The same bit is used to give a reset signal to the FPGA. In this case the byte must be written with the lowest bit cleared.

3.2 The dual ported RAM

All communication between VME-Bus and FEC is transfered over the dual ported RAM. The memory is organized in 32 bit wide words. The 32 kBytes are accessible in the address space from the long word addresses 0x0000 to 0x1fff relative to the base address of the FEM.

The two highest addresses, 0x1ffe and 0x1fff, have a special function. They can be used as mailboxes. The address 0x1ffe generates an interrupt to the FEC when written from the VME-Bus, the address 0x1fff can generate an interrupt to the VME-Bus when written by the FEC. The interrupt is cleared when the address is read by the side to which the interupt was sent.

These two addresses are used as Command and status register for the FEC. The command register at 0x1ffe is read out by the FEC immediately after it was written to by the VME-Bus. The status register is written by the FEC. It's possible to generate an interrupt to the VME-Bus each time the status register changes.

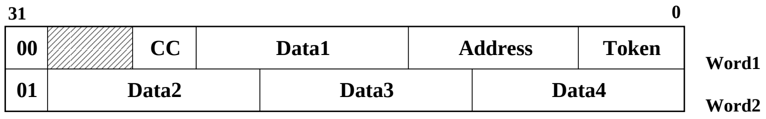

Figure 2: Format of the readout words

3.3 Programming the FEC

The FEC is controlled by commands written to the dual ported RAM. All commands are 32 bit wide. They contain a 4 bit token for identification of the command. The remaining space holds data as arguments if necessary.

There are two ways of executing commands, either immediate execution via the command register or execution of successive commands written to the memory as program.

A command written to the command register is executed immediately, independent of the status of the FEC. Since writing to the Command Register via VME-Bus generates an interrupt to the FEC, it is required to write the command as 32 bit word to ensure correct data.

Programs, build of FEC-commands, can be written to the memory. Program execution is started by an appropriate command written to the command register. In this case the FEC reads the commands sequence starting from a defined address and executes them. The program can be placed at arbitrary addresses in the memory. Also unconditional branches are possible by including a command that changes the program counter in the program.

3.4 Configuration and Readout of the FeAsics

The FeAsics are configured over the serial interface to the FEC. 23 bit words are shifted to the FeAsics. It exists a FEC-command with a 23 bit FeAsic word as argument which is sent to the FeAsics. The data is simultanously given to all four FeAsics on the FEM. It is possible to mask out one or more FeAsics if necessary.

The readout of the FeAsics uses the same serial interface as for the configuration. Data is read out in 23 bit words at a time. Data from all four FeAsics is combined in two 32 bit words and written to the dual ported RAM. To distinguish the two different words they are flagged by different values of bit 30. The format of the readout words is defined in figure 2, the meaning of the individual entries is given in table 2.

The data word from the FeAsic contains 10 bit of actual data, an 8 bit internal address and a 5 bit token identifying the mode in which the FeAsic runs. Normally the four FeAsics should run synchronously. This means token and address should be identical for all FeAsics. The FEC performs a consistency check and puts the token and address to the readout words only once and adds the information about the cross-check. A value of 1 of the corresponding cross check bit means that the compared FeAsics run synchronously.

The FeAsic can run in two modes of readout. In stop mode the digital pipeline memory is stopped and read out. In continuous readout the data is copied from the derandomizer buffer of the FeAsic and read out until stopped by an explicit command. The address is configurable to which the data is written in the dual ported RAM. There exist two different frames in the memory. They are memory regions with configurable length. Their start and end addresses can be arbitrary addresses in the address space between 0x0000 and 0x1ffd. They are set by FEC-commands.

In stop mode only the first frame is filled with data from the start address on. When the address counter reaches the end address readout stops. To read out the complete pipeline memory of the FeAsic the frame must be configured to exactly have the length to store the amount of data produced by a readout of the pipeline memory.

Readout Word 1

Bit	Description
31	0 for identifying word as readout word
30	0 for identifying readout word as word 1
29-26	Unused
25	Cross check FeAsic 3 versus FeAsic 4
24	Cross check FeAsic 1 versus FeAsic 3
23	Cross check FeAsic 1 versus FeAsic 2
22-13	Data from FeAsic1
12-5	Address
4-0	Token

Readout Word 2

Bit	Description
31	0 for identifying word as readout word
30	1 for identifying readout word as word 2
29-20	Data from FeAsic 2
19-10	Data from FeAsic 3
9-0	Data from FeAsic 4

Table 2: Content of the readout words

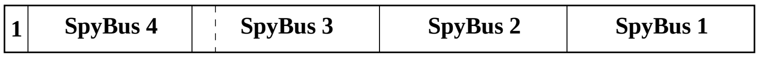

Figure 3: Format of the SpyBus word

In continuous mode the two frames are written alternately. Over the status register of the FEC it is signalled wheather a frame was completely written. It is possible to read out one frame over the VME-Bus while the other frame is written by the FEC. A continuous readout can be achieved if the VME-Bus reads data at least as fast as the FEC writes it.

3.5 Readout of the SpyBus of the FeAsic

The FeAsic has a 8 bit wide control output which allows inspection of several internal registers. The FEC can read out this so called SpyBus. The internal registers can change their values with the full clock frequency. At this speed it is impossible to write the data to the memory. It exists an operating mode in which the FeAsics receives its clock from the FEC. In this mode it's possible to run the FeAsic asynchronously to the remaining system at the speed at which FEC can write the SpyBus data to the dual ported RAM.

The readout of the SpyBus runs parallel to any other operation of the FEC and FeAsics. The SpyBus data is inserted between the other read out data. For distinction the different types of data are flagged by different values of bit 31. The four bytes from the SpyBuses of the four FeAsics are combined to a single 32 bit word. If the information in the highest bit of the SpyBus byte from FeAsic 4 is needed, it must be mirrored to the highest bit of the byte from FeAsic 3, because the highest bit of the 32 bit SpyBus word is used for distinction from the SpyBus word from the readout words. Figure 3 shows the format of the SpyBus word, table 3 gives the meaning of the individual entries.

SpyBus Word

Bit	Description
31	1 for identification of SpyBus word
30-25	Bit 6 to Bit 0 of SpyBus of FeAsic 4
24	Bit 7 of SpyBus of FeAsic 4 or FeAsic 3
23-16	Bit 6 to Bit 0 of SpyBus of FeAsic 3
15 - 8	SpyBus of FeAsic 2
7-0	SpyBus of FeAsic 1

Table 3: Content of SpyBus word

Name	Mnemonic	Binary Format
StartInput	STAI	`0001 xxxx xxxx xxxx xxxA AAAA AAAA AAAA`
LoadAddressReadout1	LAR1	`0010 xxBB BBBB BBBB BBBA AAAA AAAA AAAA`
LoadAddressReadout2	LAR2	`0011 xxBB BBBB BBBB BBBA AAAA AAAA AAAA`
StartReadoutStop	STARS	`0100 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
StartReadoutCont	STARC	`0101 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
Data	DATA	`0110 xxxx xDDD DDDD DDDD DDDD DDDD DDDD`
Readout	READ	`0111 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
StopReadout	STOR	`1000 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
StRegReset	STRES	`1001 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
SyncReset	SYRES	`1010 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
SetControlRegister	SETCR	`1011 xxxx xxxx xxxx xEEL TTTT SCCC SGDG`
StopInput	STOI	`1100 xxxx xxxx xxxx xxxx xxxx xxxx xxxx`
Wait	WAIT	`1101 xxxx xxxx xxxx DDDD DDDD DDDD DDDD`
SetMask	MASK	`1110 xxxx xxxx xxxx xxxx xxxx xxxx MMMM`
SetListenFlag	LISTEN	`1111 xxxx xxxx xxxx xxxx xxxx xxxx xxxL`

Table 4: Binary format of the FEC-commands. x means unused bit. All other letters meean bit is used as argument. See text for description.

3.6 Generating additional *Level1Accept* signals

To provide a facility to test the FEM at high trigger rates and independent to other modules, the FEC is able to generate additional *Level1Accept* signals at a configurable frequency.

3.7 The Front End Controller Commands

This section gives a complete description of all existing commands for the FEC. They are ordered in functional areas. Table 4 shows the binary format of the commands. It is shown which token belongs to which command and which bits of the 32 bit word are occupied by arguments. Also a mnemonic usable as abbreviation is given for each command.

3.7.1 Setting of address counters

LoadAddressReadout1 Set the first frame in the memory into which readout data in stop mode and continuous mode is copied. The command has two arguments, start and stop address of the frame. The addresses are in the range from 0x0000 to 0x1ffd. The default values after startup and reset are both 0x0000.

LoadAddressReadout2 Set the second frame in the memory where readout in continuous mode goes to. Two arguments are given to this command, start and stop address of the frame.

These are addresses in the range from 0x0000 to 0x1ffd. The default values after startup and reset are both 0x0000.

3.7.2 Readout

StartReadoutStop Start stop mode readout of FeAsics. Data is written into the memory region set with command *LoadAddressReadout1*. Readout is stopped as soon as all words of the memory region are written to.

StartReadoutCont Start continuous readout of FeAsics. Readout data is alternately written to the two memory regions set with the commands *LoadAddressReadout1* and *LoadAddress-Readout2*. Continuous readout is stopped with the command *StopReadout*.

Readout Read out one FeAsic word and write the two produced readout words to the memory. It is written to the address following the last written readout word. If no readout words have been written before, it is written to the address specified as start address with the command *LoadAddressReadout1*.

StopReadout Readout is stopped.

3.7.3 Input to FeAsics and control of program execution

StartInput The execution of commands is started at the memory location given by the argument which is a address in the range from 0x0000 to 0x1ffd. Data for input to the FeAsics is written at the memory as part of a FEC program using the command *Data*. The default value of the input address counter after startup and reset is 0x0000.

StopInput The execution of commands from memory is stopped.

Wait Wait for a specified number of clock cycles. If the FEC is in this waiting state no other commands are executed, even if they are written to the command register. This is the only condition under which execution of commands written into the command register is delayed by more than one memory access cycle.

The command takes an 16 bit argument which is loaded into an internal counter. This counter counts up with the internal operating frequency of the FEC. It stops when it reaches the value 0xffff. Then the FEC returns to normal operation.

Data This commands takes a 23 bit data word as argument which is shifted as input data to the FeAsics via the serial interface.

SetListenFlag The Listen flag which controls the direction of the serial interface between FEC and the four FeAsics is set to the value of the lowest bit of the argument.

A negative edge of the Listen flag starts the internal playback memory of the FeAsic.

3.7.4 Reset of the FeAsic

StRegReset Send a StRegReset signal to the FeAsics. The Listen flag must be 1 for the reset to take place.

SyncReset Send a SyncReset signal to the FeAsics. The Listen flag must be 1 for the reset to take place.

Bit	Name
14	EnableFeClk
13	EnableStatusWrite
12	Light
11-8	TriggerDelay
7	SpyBusEnable
6-4	SpyBusCtrl
3	SwapBits
2	GenerateTrigger
1	DisableTrigger
0	GLinkHalt

Table 5: Segmentation of the FEC Control Register

3.7.5 Configuration of FEC

SetControlRegister The internal Control Register of the FEC is set. This register controls the features of the FEC which do not belong directly to input and readout of the FeAsic. The command takes an 15 bit argument which is written to the register. Table 5 lists the meaning of the individual sections of the argument. For single bits a value of 1 means active status.

If *EnableFeClk* is active the FEC provides the clock for the FeAsics. Its frequency is the same as the frequency the FEC is operated with unless bit *SpyBusEnable* is active. In this case the clock for the FeAsics is asynchronously controlled by the FEC.

The *EnableStatusWrite* bit controls if the FEC writes to the status register in the dual ported RAM. Default value is 0. The status register is not updated until explicitly allowed by setting this bit of the control register.

The *Light* bit controls a LED at the front panel of the FEM. This LED can be switched on and off by commands to the FEC. It can be used to give a quick impression whether the FEC is at life.

Generation of trigger signals is controlled by the bit *GenerateTrigger*. In case *DisableTrigger* is active, external *Level1Accept* signals are not given to the FeAsics. The four bits of *TriggerDelay* give the period of the additional generated Level1Accept signals in the following way. The most significant 4 bits of an 8 bit counter are loaded with the value of *TriggerDelay*. The counter counts up until it reaches the value 0xff. Then a Level1Accept signal is generated and the counter is loaded with *TriggerDelay* again. This continues until *GenerateTrigger* is deactivated.

The bit *SpyBusControl* controls if the SpyBus of the FeAsics is read out. If it is active the clock which operates the FeAsics comes from the FEC asynchronously to the system. SpyBus data is written additionally to the memory. In order to mirror bit 7 of the SpyBus byte of FeAsic 4 to bit 7 of the SpyBus byte of FeAsic 3 *SwapBits* must be active.

The two G-Link chips on the FEM can be stoped by setting bit *GLinkHalt*.

SetMask This command controls which FeAsics are active for input and readout. The argument of this command is a 4 bit value loaded into a register of the FEC used as mask for the FeAsics. This is done by combining the handshake signals of the serial interface of the FeAsic with the mask by an AND. Data is shifted through the inactive FeAsic but it is not acknowledged if the corresponding bit in the mask is not set. The most significant bit of the argument belongs to FeAsic 4. The other FeAsics follow in descending order.

Bit	Name
31-27	*Unused*
26-12	Control register
11-8	Mask
7	*Unused*
6	Light
5	Frame2Done
4	Frame1Done
3	Frame
2	Continuous
1	ReadoutActive
0	InputMode

Table 6: Content of the status register

3.8 The status register

Information about the status of the FEC is collected in the status register. It is written to the 32 bit word at address 0x1fff of the dual ported RAM. It contains the control register of the FEC, the mask register which selects the FeAsics being accessed and some signals reflecting the status of the readout. These signals are contained in the lowest byte of the status register. The status register is only written to the status register if this byte changes and *EnableStausWrite* of the control register is active. Writing can be forced by toggling the *Light* of the control register. It is possible to generate an interrupt to the VME-Bus each time the status register is written to the dual ported RAM. In table 6 the meaning of the bits of the status register is listed. A value of 1 means, unless otherwise stated, that the corresponding function is active.

Over the bits *Frame2Done* and *Frame1Done* it is signaled that the memory regions set by the commands *LoadAddressReadout1* and *LoadAddressReadout2* are filled and data is ready for readout over the VME-Bus. The value of *Frame* gives the currently written region, 0 means Frame 1, 1 means Frame 2.

The bits *Continuous* and *ReadoutActive* reflect the status and mode of the readout. If *InputMode* is set, commands are read from memory pointed by the program counter, which can be set by the command *LoadAddressInput*.

The *Light* bit is mirrored from the control register.

4 The FeAsic

(to be filled)