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4-channel FADC : Technical Specification

1. SINGLE-WIDTH VME SLAVE MODULE: General Features

The VME-board is a STANDARD VME-slave-module, accessed from the Master by memory-mapping. Optionally, 16-bit or 32-bit data-transfers on the VME-bus must be selectable (32-bit = Longword-access). The module shall contain FOUR FADC-channels of 8-bit resolution, capable to digitise the analogue input signal with a sampling rate of 100 MHz. All 4 channels are driven by a continuous, external clock.

Each FADC-channel is equipped with a scrolling memory (256 bytes long covering 6.4 µsec @ 40 MHz). The memories shall record the FADC-results in a circular manner while a common Digitisation-Gate (D-GATE = 1) is present. Their contents are frozen by an external STOP (D-GATE = 0), which is normally induced by a "YES" from the "Cluster-Finder-Logic". VME-access to the memories is permitted only when digitisation is stopped.

During Digitisation, the module transports the FADC-data (4 bytes) in real time to its front panel connector.

The module must also allow data- Playback from the memories to the front panel connector. This requires WRITE-access from the VME-bus to load data. Playback shall also be driven by the same external clock.

1.1 FRONT PANEL

4 Lemo-sockets for analogue signal inputs (50 Ohm terminated, >=30 nsec rise-time).

Provision shall be made for reconfiguration of the receiver in future, to accept also balanced signals of similar rise-time.

2-pin Connector for ECL-CLOCK (In)
2-pin Connector for ECL-STOP (In)
2-pin Connector for ECL-SYNC_CLOCK (Out)

64-pin IDC-type (e.g. 3M with clamp) Connector for FADC-output; 4 bytes = 32 bits balanced (ECL for immunity to distance) with Pin-layout as defined in "Revised FP-Connector".

LED for CLOCK (continuously ON, when Clock present).
LED for STOP (ON when STOP, i.e. D-GATE = 0 from front panel .OR. software).

LEDs for Supply Voltages ("AND" of all required Voltages).

2. Specification for ONE FADC-channel:

2.1 INPUT LINE RECEIVER:

The Line-receiver has to accept a bipolar (negative - positive overshoot) analogue signal from LAr-Calorimeter (i.e. summed Shaper output). The percentage of negative-to-positive amplitude for the bipolar pulse is approx. 90% over 10%.

The Line-Receiver should be reconfigurable for differential signals; i.e. implementation on piggy-back(!).

ALSO: An Amplifier with NON-LINEAR (e.g. logarithmic) characteristics could be used here in future, to increase the dynamic. range for triggering.

The input signal must be INVERTED and an appropriate DC-OFFSET (-2.5 V) applied, to map the Signal into the acceptance-window of the FADC (-2.5 to 0 Volt).

A DC-bias must shift the positive part of the LAr-signal into the FADC-window to have this part digitised as well. This Bias is adjustable (e.g. to 10% = 0.25 V) on board (VME-writeable DAC, common for all four FADC-channels).

Hence, the maximum input signal-amplitude, that yields a FADC-value = FF is -2.25 VOLT (Negative part corresponds to dynamic range for trigger-thresholds; positive part amounts to ca. +0.25 Volt=10%).

2.2 FADC Chip:

The proven (RD33) AD9012 (100 MHz capability) can be used.

It must be ensured that FADC-overflow (no matter how big the input signal) yields a "YES", i.e. Data = FF must be present for positive signals exceeding the input-range.

2.3 MEMORY:

The memory/channel is 256 bytes long. It must be capable to "store-away" and "play-back" 8-bit FADC-values at 10 nsec intervals, for which the addresses are generated by a revolving counter. The counter is stepped by the external clock.

The Address-counter is VME-readable to obtain the STOP-pointer.
The Address-counter must also be VME-writeable to set a start- and stop-address for Readout (e.g. partial Readout).

VME-ERRORS must NOT lead to "hang-ups", but raise an ERROR-flag in the Control-register.

3. REAR Connectors to VME-Backplane:

>>> J1 is the Standard 96-pin DIN Connector for a 16-bit VME-bus.

>>> J2 is the USER-connector, of which the central (B) row is used for 32-bit VME-transfers (32-bit VME-extension).

4. VME Access

4.1 DATA-memories: (READ/WRITE)

One time slice yields 4 Data-bytes (1 byte/FADC-channel). Those four bytes are grouped into ONE 32-bit word for VME-operations, i.e. FADC#0 == LS Byte ... FADC#3 == MS Byte.

Memory reading in a Data-Acquisition system must be possible in block-transfer mode (DMA); not only by single word access !!!

For optional 16-bit VME-access, the address-mapping should select two groups of FADCs,
First Data-word : FADC#0,FADC#1
Second. Data-word: FADC#2,FADC#3

>>> VME-Addressing (i.e. Offsets from Base address) is to be fixed YET !

4.2 Control/Status Register: (16-bit register: READ/WRITE)

bit#0: 1= Ext. Clock detect (check presence of 0-1 transitions;
stretch 100 msec; i.e. always set when CLOCK-frequency >10 Hz)

bit#1: Digitisation status (reflects D-GATE input):

1= Digitisation (needs bit#0=1; otherwise ERROR)
0= other MODES (VME-access)

bit#2: D-GATE source control:

1= D-GATE from front panel (P-up default)
0= D-GATE from Software (VME, overruns front panel when
VME-access is allowed, i.e. D-GATE=0 from front panel .OR.disconnected.)

bit#3: MODE selection:

1= Playback (needs bit#0=1; otherwise ERROR)
0= VME-access (READ/WRITE)

bit#4: Software D-GATE:

1=ON (needs bit#3=1; starts Playback)
0=OFF (stops Playback)

CAUTION : Starting Playback simultaneously for ALL FADC-boards can ONLY be done by external D-GATE from front panel !!! Playback from Individual. FADC-modules for tech. tests should also be possible by software control. Playback always takes place in circular manner (i.e. like "inverse recording").

bit#6: VME-ERROR status:
1= Any sort of VME-ERROR occurred (accumulative)

bit#7: ERROR status:
1= Missing Clock

bit#8 -> bit#15 : RESET (to 0) bit#0 -> bit#7

5. Main Operating MODES:

Real-Time digitisation: data to front-panel connector and circular memory during open time of Digitisation-Gate [0-1 edge: START; 1-0 edge STOP]. The driving clock may run on continuously.

Playback of recorded (or VME-written) digitised data to front panel connector driven by external clock.

VME-access (READ/WRITE), when digitisation is stopped by D-GATE from front panel (or disconnected).

TABLE of Control for Operating Modes:

MODE bit#	0	1	2	3	4	5	6	7
Digitisation of analogue Input Signals		1	1	x	x		?	?
VME Readout	x	0	0	0	0		?	?
VME Write to FADC-memories	x	0	0	0	0		?	?
Playback:ext.D-GATE i.e.ALL FADCs simultaneously	1	0	1	1	x		?	?
Playback:D-GATE from SW i.e.Individual.FADC-module	1	0	0	1	0 1 0		?	?
i.e.Individual.FADC-module								

6. Additional Notes

The feedback resistor on the Line-Receiver piggy-back will be implemented as a "wire-resistor" with plated-through holes (NOT a SMD-resistor). This allows reasonably easy change of the gain by a factor 2, to map a 0 - 1 Volt range into the FADC-window instead of the foreseen 0 - ca.2 Volt range.

Front panel space is now rather limited on this FADC-module. I propose to leave the CLOCK- and D-GATE- Inputs as 2-pin ECL-connectors instead of having NIM-Lemo-Sockets plus converters on board. I propose further to build (us at Heidelberg) ONE "stupid" VME-board, which does the following:

CLOCK: One NIM-input, convert, 16 ECL-outputs (Fanout).

D-GATE: One NIM-input, convert, 16 ECL-outputs (Fanout).

This Fanout-module sits in the same VME-crate together with the 9 FADC-modules. We (Heidelberg) provide the necessary single twisted-pair cables of equal length, to take the signals from the Fanout to the individual FADC-modules. (Standard practice since years in the ALEPH-L1-trigger for e.g. STROBE-distribution.)

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7. Internal Addressing of FADC-module

Each FADC-module decodes the VME-address bits A00-A23. The Address-modifier is either 39 (single-cycle access) or 3B(DMA block-transfer mode).

The modules, containing 4 FADC-channels each, are accessed on the address-segment C1 (coded in a GAL and therefore exchangeable, if need arises in a larger system). On each module five bits are decoded by a "jumper-array" to identify the individual module, i.e. max. 32 modules can be addressed.

7.1 Module-addressing:

C1 00 xx -> module#0

C1 09 xx -> module#9

C1 1F xx -> potential module#32

Each module has an internal address space of 256 addresses
Address-bit A7=0 controls the VME Read/Write operations, whereas A7=1 alone accesses the Control/Status register.

7.2 Functional addressing of a module:

xx = 80	R/W	Control/Status register: significant DATA:	D0-D7 Word
xx = 00	R/W	Memory chan.1-chan.4: when in VME 32-bit mode	Longword
xx = 00	R/W	Memory chan.1-chan.2: when in VME 16-bit mode	Word
xx = 02	R/W	Memory chan.3-chan.4: when in VME 16-bit mode	Word
xx = 04	R	Memory-address Counter: significant DATA:	Word D0-D7
xx = 04	W	Memory-address Counter: significant DATA:	Word D8-D15
xx = 06	W	Offset-DAC: significant DATA:	Word D0-D7

8. Bit-content of Control/Status register (xx = 80):

8.1 WRITE:

D0 unused

D1 unused

D2 Source of Digitisation Gate 0= Internal from Program, 1= External from Front panel (Default)

D3 Running Mode 0= Record, 1= playback

D4 Internal Dig. Gate 0= Off, 1= On

D5 unused

D6 Reset Program Error 1-0

D7 Reset Clock Error 1-0

8.2 READ:

D0 Clock Status 0= Missing Clock, 1= Clock (>10Hz) detect

D1 Status of ext. Dig. Gate 0= Off, 1= On

D2 BUSY status 0= Off (comprises Record and playback) 1= On

D3 Run Mode status 0= Record, 1= playback

D4 Int. Dig. Gate status 0= Off, 1= On

D5 unused

D6 Programming Error status 0= Off, 1= On

D7 Clock Error status 0= Off, 1= On