Level-1 Trigger Complete Slice Test 1997

ID	Task Name	Duration
1	**JET PROCESSOR**	**95d**
2	Design	4w
3	Schematic Capture	2w
4	Layout	2w
5	PCB Manufacture	3w
6	Assembly	1w
7	Testing	3w
8	Integration with DAQ	4w
9	Diagnostic S/W Dev	6w
10	DAQ S/W Dev	3w
11		
12	**FRONT-END MODULE**	**45d**
13	Manufacture PCB(3 off)	2w
14	Assembly (2 off)	1w
15	Power & VME TEST	10d
16	Test and Integrate at RAL	4w
17	DAQ S/W Dev	4w
18	Test at Heidelberg	4w
19		
20	**CTP DEMONSTRATOR**	**70d**
21	Board Tests	4w
22	Detailed Hardware tests	8w
23	Move Cern DAQ to West /	1d
24	DAQ S/W Dev	4w
25	Integrate with DAQ	2w
26		
27	**BEAMLINE**	**47d**
28	Installation & Cabling	3w
29	Beam Running - Tile 1	2w
30	Beam Running - Tile 2	2w