Project Specification

Project Name: LHC Calorimeter Trigger,
ATLAS Transmitter Module Demonstrator Phase 2

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Approval	Name	Signature	Date
Author	G.C.Lewis		
Project Manager	V.Perera		
Customer	A.R.Gillman		

Distribution for all updates:

Project Manager: V.Perera
Project Engineer: G.C.Lewis
Customer: A.R.Gillman
Group Leader responsible for Project: S.P.H.Quinton
Project Managers of related projects:

Additional distribution at PDR and FDR:

System Design Group Leader:
Micro Electronics Design Group Leader:
Design Support Group Leader:
Management Support Services Group Leader:

1. Scope

This project is part of the ATLAS level 1 calorimeter trigger system Phase II demonstrator. The data transmission chain consists of four parts:

1—Analogue to Digital Module (ADM)
2—Transmitter Module (TXM)
3—Cluster Processor Module (CPM)
4—Timing Controller Module (TCM)

Analogue data from the calorimeter is digitised by the ADM and passed to the TXM for transmission to the CPM via optical fibre and coaxial cable for further processing. The TCM supplies the clock signals to all the modules so that the flow of data along the pipeline is fully synchronous.

2. Related projects and documents

The Transmitter Module includes the Bunch Crossing Identification (BCID) Algorithm implemented in a Xilinx 4008 FPGA.

The Analogue to Digital Module contains the FADCs designed and built at Heidelberg which transmit the data to the Transmitter Module.

Relevant Documents

- *Phase 1 Demonstrator BCID Card Programming Model,* Jason Leake, 5/5/95
- *System Specification for the Level-1 Calorimeter Trigger Demonstrator Phase 2*, A R Gillman, 24/3/95
- *Functional Specification for the Level-1 Calorimeter Trigger Demonstrator Transmitter Module*, E Eisenhandler, A R Gillman, 26/3/95
- *4-Channel FADC : Technical Specification (AMD Design Specification)* 12/94
- *CPM Design Specification*: Draft, 26/6/95
- Hewlett Packard Low Cost Gigabit Rate Transmitter/Receive ChipSet Technical Data
- Finisar FTM/FRM-8510 Fiber Optic Transmitter/Receiver Technical Data
- *Finisar Application Note: Interfacing Various Gb/s Chip Sets* (Ref: AN-2012 7/94)
- *Finisar Application Note: Using the Built-in Test/Diagnostic Port* (Ref: AN-2010 2/94)
- *Finisar FDB-101X Simplex/Duplex Optical Module Evaluation Boards* (Ref: AN-2010)

3. Technical Aspects

3.1 Requirements

The Transmitter Module functionality will be split between a Mother Board and a Daughter Card both of which will be a 6U VME cards (J1, J2), this will result in a double width module Each Module is to receive 4 channels of 8-bit data from the Analogue to Digital Module in balanced ECL. The following functions are required to be performed on each channel of the received data:

- Pedestal subtraction and calibration. **(Mother Board)**
- Bunch Crossing Identification (BCID). **(Mother Board)**
- Serialisation in pairs of channels. **(Daughter Card)**
- Optical transmission. **(Daughter Card)**
- Electrical transmission. **(Daughter Card)**
- Test mode, in which simulated data is fed into the system just before the BCID stage

The data for each channel is required to be transmitted serially in both electrical and optical format. The optical format is to drive approximately 80 metres of fibre optic cable and the electrical is to drive approximately 2 metres of 75 ohm coaxial cable.

The data pipeline through the Transmitter Module will be accessible when the data pipeline is not active, at two points VME D32:D16 via the input and output memories (see TXM block diagram). There will be no D8 access.

Board layout needs to take into consideration the replacement of the Xilinx 4008 FPGA with the Heidelberg daughter board.

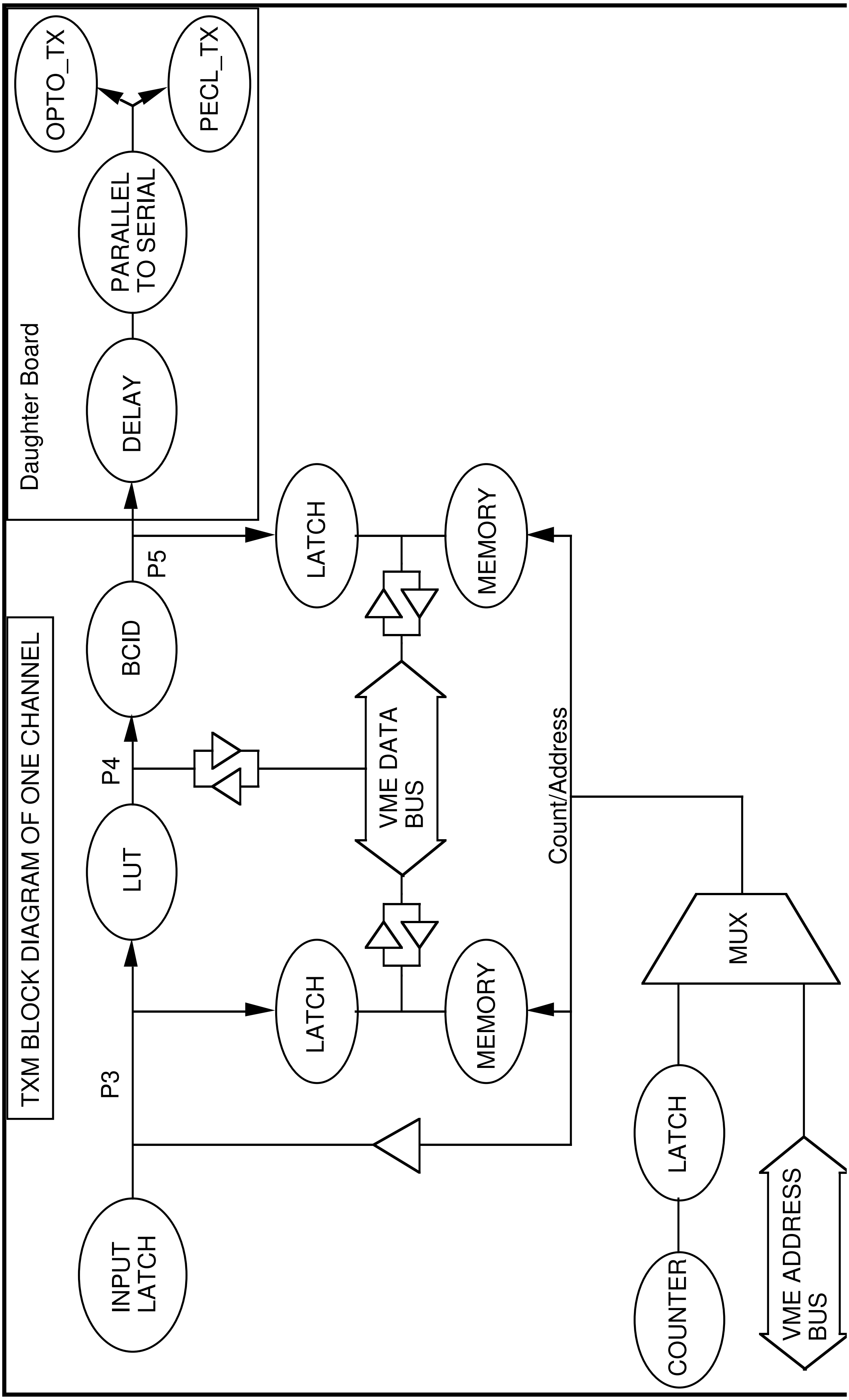
TXM BLOCK DIAGRAM OF ONE CHANNEL
Daughter Board
INPUT LATCH
P3
LUT
P4
BCID
P5
DELAY
PARALLEL TO SERIAL
OPTO_TX
PECL_TX
LATCH
MEMORY
LATCH
MEMORY
VME DATA BUS
Count/Address
MUX
LATCH
COUNTER
VME ADDRESS BUS

Diagram 1

3.2 Specification of deliverables

3.2.1 Functional Stages of Pipeline

Functions 1-5 are performed on a Mother Board and functions 6-9 are performed on a Daughter Card.

1. Input: 4 channels of 8-bit balanced ECL.

2. Logic level conversion: ECL to TTL.

3. Data capture: Latches input data.

4. Pedestal subtraction and calibration: RAM Lookup Tables (**LUT**), 256*8 per channel.

5. Bunch Crossing Identification: Performed by the proven **BCID** algorithms, a single Xilinx 4008 FPGA is required for 4 channels.

6. Programmable delay: To enable a full 36-channel system to cope with differences in transmission time for electrical and optical links.

7. Logic level conversion: TTL to PECL.

8. Serialisation: Two 8-bit data channels will be converted into a serial data stream using the Hewlett Packard HDMP-1012 Gbit/s Link (G-link).

9. Transmission: The data is to be transmitted via two methods:

    Optically along a multi-mode fibre for approximately 80 metres using a Finisar FTM-8510-1.

    Electrically using PECL along approximately 2 metres of coaxial cable.

3.2.2 Input and Output Monitor Memories

The data in the Transmitter Module pipeline will be spied upon at up to 45 MHz by monitoring memories. These barrel store memories will be 256 bytes per channel and constantly scrolling. They will monitor the data at the input just after the input latches and at the output just after the BCID algorithm has been applied.

3.2.3 Programmable delays

The delays enable a full 36-channel system to cope with differences in transmission time for electrical and optical links. Coarse and fine delays are required see the programming model, section 3.3 of this document, for more detail.

	Range	Resolution
Coarse delay for **BOTH** pairs of channels	30 clock periods (i.e. 750 ns at 40 MHz system clock)	1 clock period (25 ns at 40 MHz system clock)
Fine delay for **EACH** pair of channels	1 clock period (5 bits) (i.e. 25 ns at 40 MHz system clock)	1 ns

3.2.4 Timing signals

Two clocks are provided to the Transmitter Module, a system clock (*SYSCLK*) and a dedicated G-Link clock (*GCLK*) that will normally run at the system clock frequency, with the option of running at twice the system clock frequency (*SYSCLK* x 2).

The system clock (*SYSCLK*) is obtained as a balanced ECL input on the front panel. This is a free running clock, equivalent to the LHC clock, which is phase locked to clocks supplied to the Analogue to Digital Modules and the Cluster Processing Modules, so that for each clock cycle the data advances by one stage through the processing and transmission pipeline.

For the purpose of demonstration the system clock of 40 MHz shall be driven up to 45 MHz (~40 MHz + 10%) to explore tolerance to clock frequency.

The separate G-Link clock (*GCLK*) has the option of running at twice the system clock (*SYSCLK*) frequency (i.e. 80—90 MHz) to explore the upper frequency range of the G-link chipset. At 40 MHz the G-link will convert a 16-bit parallel word into a 20-bit data stream (16-bits of data plus 4 control bits) which results in 800 Mbaud. To double the baud rate to 1.6 Gbaud the clock fed to the G-link has to be doubled to 80 MHz. Note that the rest of the Transmitter Module will always use the system clock (*SYSCLK*).

The module can also be operated in the absence of a Timing Control Module (TCM) in two ways. It can either be driven using an internal 40 MHz test clock, or the BCID stage may be single stepped in Test mode.

A *STOP* signal is produced by the Timing Control Module a short time after a beam trigger. It prevents the Transmitter Module from responding to the System Clock (*SYSCLK*) signal, hence stopping the scrolling monitoring memories in preparation for readout over VME.

3.2.5 Front Panel Input and Outputs

3.2.5.1 Front Panel Inputs

Description	Logic	Connector	Termination
Data Channel 0-3	Balanced ECL	64-PIN IDC	100 ohm
System Clock (≤ 45 MHz *SYSCLK*)	Balanced ECL		100 ohm
G-link Clock (≤90 MHz *GCLK*)	Balanced ECL	10-PIN IDC	100 ohm
STOP signal	Balanced ECL		100 ohm

3.2.5.2 Front Panel Outputs

Transmission Data Rate for **all** output Data Channels is 800-1600 Mbaud

Description	Logic	Connector	Termination
Data Channels 0-1 Data Channels 2-3	Single ended ECL Single ended ECL	SMB SMB	75 ohm 75 ohm
Data Channels 0-1 Data Channels 2-3	Optical Optical	ST ST	

3.2.8 Front Panel Monitoring (LEDs)

The LEDs are located at the top of the front panel, to prevent obstruction by dangling cables.

Description	Signal name	Colour
+5 Volts (Mother Board)		Green
-5 Volts (Mother Board)		Green
+5 Volts (Daughter Card)		Green
+5 Volts (Daughter Card)	Finisar Power Supply	Green
Card is Halted *(i.e. Card is Halted* set)	*HALT*	Yellow
Programming error (i.e. *Error* set)		Red
VME access in progress		Yellow
FPGA loaded (i.e. *Done* set)	*DONE*	Green
Optical output active		Yellow
System clock is active	*SYSCLK*	Green
G-Link clock is active	*GCLK* (Daughter Card)	Green
Test clock is active (i.e. *Test Clock Enable* set)		Red

Short pulsed signals such as Card is Halted and VME Access will light the LEDs for long enough to be seen.

3.2.9 Rear Panel Input and Outputs

1) VME J1 Connector
2) VME J2 Connector

3.2.10 Power Requirements

Voltage rail	Estimated Max. Current
+5V +12V	5 A 1A
-12V	1 A

Estimated Power to be dissipated is 20-30 Watts.
The -5V supply will be generated from the -12V supply.

3.2.11 Test and Set-up Points

3.2.11.1 Logic Analyser Probe Points

There will be logic analyser probe points on various data paths to aid in the debugging of the Transmitter Module.

3.2.11.2 Data/Clock Set-up Points

The arriving data is required to be set-up in relation to the system clock (*SYSCLK*), so that it will be reliably latched into the Transmitter Module. To aid this setting-up the

Least Significant Bit (LSB) of each channel and the clocking signal for the input latches should be accessible. The clocking signal for the input latches is derived from the system clock (*SYSCLK*).

3.2.11.3 Ground Points

Ground points will be provided for scope probe grounding.

3.3 Transmitter Module Programming Model

3.3.1 Guidelines

These are to aid the software control of the module.

1. All registers can be read by the computer, hence there are no 'write only' registers. The register bits generally have the same meaning for reads as for writes.

   All Status Registers shall be Read-Only registers.

   All Control Registers shall be Read/Write registers.

   Reading back a register will generally return the last value written.

   Attempts to write to read-only registers or undefined portions of registers will result in the non-modifiable fields being left unchanged. Fields such as *Generate Single Tick* bit in the *TXModule Control Register* can be used to repeatedly trigger an operation by repeatedly writing a 1 to them. In such cases, they will always read back as 0.

2. It is illegal for the computer to read or write a value which the Transmitter Module itself is able to modify at the same time. Therefore when the pipeline is active, (i.e. the *Card is Halted* will be 0 in the *TXModule Control Register*) so that the free-running external 40 MHz Clock is being accepted, the computer cannot legally access most of the registers on the TXM.

3. When the used area of the 64 kilobyte address space occupied by the Transmitter Module is addressed, it will always respond with a handshake to avoid a bus error.

4. The power-up condition of all registers will be all zeros, unless otherwise stated.

3.3.2 Notation

The names of the registers and bit fields within them are written in *italic*. The names of the signal lines are *underlined italic*. Bit fields are labelled Input to Card and Output from Card rather than Write and Read to make it clear whether it is the card or the computer which is doing the writing.

In this document, a byte is always an 8 bit field, a word is always 16 bits and a long-word is always 32 bits.

Setting a bit field means writing a 1 to it, clearing it means writing a 0.

3.3.3 Memory Map

The Transmitter Module is addressed using an A24 address bus. It uses the 16 least significant bits of the A24 address bus, hence the address space of the Transmitter Module is 16-bits. This corresponds to 64 kilobytes per module. The 8 most significant bits of the address can be pre-set by switches to allow the 64 kilobyte memory space required to sit at any convenient 64 kilobyte boundary within the 16 megabyte A24 address space.

Byte Address (hex)	Register type	Register Name	Size in bytes	Description
0	RO	TXModuleID	2 (16 bits)	Type, serial number & revision
2	RW	TXModuleCR	2 (16 bits)	TXModule Control Register
4	RO	TXModuleSR	2 (16 bits)	TXModule Status Register
6	RW	XilinxCR	2 (16 bits)	BCID Xilinx Control Register
8	RW	ProgReg	2 (16 bits)	BCID Xlinx Program Register
A	RW	GLinkCR	2 (16 bits)	HP G-Link Control Register
C	RO	MemCounter	2 (16 bits)	Scrolling Memory Counter
E	RO	Error register	2 (16 bits)	Bit mask indicating reason(s) for Error bit in TXModuleSR being set
10	RW	OptoDiagnostic	2 (16 bits)	Finisar Diagnostics Register
12	RW	DELAY01	2 (16 bits)	Delay Register (Coarse/Fine)
14	RW	DELAY23	2 (16 bits)	Delay Register (Fine ONLY)
16	RO	DaughterID	2 (16 bits)	Daughter Module ID Register
18-FFF				Undefined
1000 17FF	RW	IPMem	2K (256x4x2) ‡	Input Memory RAM (Address range 000-3FF) repeated once to aid block transfer. 32 Bit Bus
1800 1FFF	RW	OPMem	2K (256x4x2) ‡	Output Memory RAM (Address range 000-3FF) repeated once to aid block transfer. 32 Bit Bus
2000 21FF	RW	LUTMem0	256	Look Up Table RAM 0 Address range 00-FF 256 x 16-Bits
2200 23FF	RW	LUTMem1	256	Look Up Table RAM 1 Address range 00-FF
2400 25FF	RW	LUTMem2	256	Look Up Table RAM 2 Address range 00-FF
2600 27FF	RW	LUTMem3	256	Look Up Table RAM 3 Address range 00-FF
2800 FFFF				Undefined

‡ The 2 kilobytes of memory address space is made up of a memory store of 256 bytes for each of the four channels, the addresses of these memories being duplicated to aid rapid transfer of data.

RO means that the computer can only read the value of this register, writing has no effect either to the value or the state of the module.

RW means that the computer can affect the state of the module by writing to this register.

All usable memory on the card is directly mapped into VME address space so as to be conveniently accessible by the computer.

The input and output memories are packed so that the read out is in time slices—i.e. the input memories for each of the 4 channel are 8-bits wide therefore a 32-bit time slice (8-bits * 4) will be created.

The module responds to the following VME Address Modifier codes.

AM code	
39	Standard (i.e. A24) non-privileged data access—All registers
3B	Standard non-privileged block transfer—Input and output memories only (D16)
3D	Standard supervisory data access—All registers
3F	Standard supervisory block transfer—Input and output memories only (D16)

3.3.4 TXModuleID Register

The Transmitter Module identification register is used to uniquely identify the module.

Register Bits	Assignment	Description
0-7	SerialNumber[0:7]	Different for each module of a given type, in sequence staring with 1.
8-10	Revision[0:2]	Different for each version of the module. Initially it is 1.
11-15	Type[0:4]	Different for each type of module. For the Transmitter Module it is always 2.

3.3.5 TXModule Control Register

All bit fields are inputs to card. Power-up condition will initially set all control register bits to 0 unless otherwise stated (i.e. *System Clock Disable* is initialised to 1).

Bit	Descriptive Name	Signal name	
0 (LSB)	*Clear Stop*	*CLRSTP*	Always 0 on read
1	*Test Mode Enable*	*TMDEN*	
2	*Clear Error*	*CLRERR*	Always 0 on read
3	*Generate Single Tick*	*TICK*	Always 0 on read
4	*System Clock Disable*	*CLKEN*	
5	*FIFO Clock Read MUX*	*FIFO_CKR_MUX*	
6	Unused		Always 0 on read
7	*Global Reset*		Always 0 on read
8	*Scrolling Memory Counter Reset*		Always 0 on read
9	*Test Clock Enable*		
10	*Opto Output Select*		
11-15	Unused		Always 0 on read

3.3.5.1 Clear Stop

Bit 0

The *Stop* bit is cleared by setting the *Clear Stop*. *Clear Stop* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Clears the *Stop* bit

3.3.5.2 Test Mode Enable

Bit 1

Setting this bit switches the module into Test mode. This allows testing of the data stream from the lookup table memories through the Xilinx and into the output memories. Test mode sets the following.

- The lookup table memory data are interpreted as test data and clocked into the Xilinx FPGA on each clock tick. The lookup table memory is normally addressed by input data, and the resulting values from the memory fed into the Xilinx FPGA. In Test mode, the lookup table is addressed by the scrolling memory counter instead. Thus, for each channel, each value in turn is presented to the Xilinx in a cyclical fashion.

- It activates the relevant parts of the pipeline even when the card is halted. This means that the *Generate Single Tick* field can be used to clock data through the Xilinx whilst the card is halted. Alternatively, the card can be clocked by the external or test clocks at full speed.

Because the pipeline around the memories is active when this bit is set, it is not possible to access the memories successfully from VME. Read attempts will return unpredictable values, and writes will have no effect. To access the memories, Test mode must be first disabled.

0	Transmitter Module is in normal beam line mode
1	Transmitter Module is in Test mode

3.3.5.3 Clear Error

Bit 2

The *Error* field in the *TXModule Status Register* and the *Error Register* are reset by writing a 1 to *Clear Error*. *Clear Error* is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Clears the *Error* bit in the *TXModule Status Register*

3.3.5.4 Generate Single Tick

Bit 3

When a 1 is written to this bit, the internal single clock tick generator emits a single pulse. This is only possible when both of the following conditions are met:

- The pipeline is inactive (i.e. when the *Card is Halted* bit is set). The easiest way of doing this is to set *System Clock Disable.* If *Generate Single Tick* is set when the pipeline is active, the result is unpredictable and the *Error* bit is set in the *TXModule Status Register*.

- *Test Mode Enable* is set. This is necessary for the various memories to be accessible for the data in the pipeline. If this is not the case, then the memories will not be changed but otherwise the results will be unpredictable.

Generate Single Tick is always read 0, and writing 0 has no effect.

0	Read value, no effect on writing
1	Pulses the internal single clock tick generator

3.3.5.5 System Clock Disable

Bit 4

If clear, this bit enables the external System Clock to be accepted into the Transmitter Module. When set, the *Card is Halted* bit is set automatically at the same time. In this state (*Card is Halted = 1*), the single tick generator can be used to clock the card.

0	Use external System Clock
1	Halt Transmitter Module, but allow use of internal single tick clock generator

Note: The **Power-up** state of the *TXModule Control Register* has *System Clock Disable* set to **1**—i.e. the external system clock is disabled. This allows the Xilinx FPGA and the Lookup tables to be loaded before the card is set running.

3.3.5.6 FIFO Clock Read MUX ¥

Bit 4

This bit is used to ensure that the FIFO delays always receive a 40MHz clock signal. When cleared the Read clock of the Delay FIFO is feed with G-Link Clock. When set the Read clock is feed by half the frequency of the G-Link clock, this is for when the G-Link clock is 80MHz.

0	G-Link clock is used to strobe the read of the delay FIFO
1	Half G-Link clock frequency used to strobe the read the delay FIFO

3.3.5.7 Global Reset

Bit 7

When a 1 is written to this bit, a single pulse will reset the Transmitter Module to a known power-up state. This is only possible when the pipeline is inactive (i.e. when the *Card is Halted* bit is set). *Global Reset* is always read 0, and writing 0 has no effect.

The same effect can be produced using the VME *System Reset**.

0	Read value, no effect on writing
1	Resets the Transmitter Module to the initial power-up state

3.3.5.8 Scrolling Memory Counter Reset

Bit 8

When a 1 is written to this bit the scrolling memory counter is reset to zero.

0	Read value, no effect on writing
1	Resets the Scrolling Memory Counter

3.3.5.9 Test Clock Enable

Bit 9

This field is used to enable or disable the driving of the system and G-link clocks by an internal 40 MHz clock. This allows the Transmitter Module to be operated at normal speed without a Timing Control Module to generate the clock signals.

0	Test clock disabled
1	Test clock enabled

3.3.5.10 Opto Output Select

Bit 10

The electrical output of the Transmitter Module will always be active. This bit will switch the optical output on or off for **both** Finisar devices.

0	No optical output. This is the default power-up state for safety reasons.
1	Optical output enabled for all channels

3.3.6 TXModule Status Register

This is a read-only register.

Bit	Descriptive Name	Signal name	
0 (LSB)	*Card is Halted*	*HALT*	
1	*Stop*	*STOP*	
2	*Error*	*ERROR*	
3	*Data Valid*	*DAV**	
4	*Control Valid*	*CAV**	
5	*G-Link Locked 0,1*	*LOCKED01*	
6	*G-Link Locked 2,3*	*LOCKED23*	
7-15	Unused		Always 0 on read

3.3.6.1 Card Is Halted

Bit 0

When set, the system clock is blocked so that it can not drive the card. The local single tick generator may still be used to drive the card, though.

The card sets this bit when either (or both) of the following conditions is detected:

1. The *System Clock Disable* bit is set to 1
2. The *Stop* bit is set to 1

When clear, only the *TXModule Control*, *TXModule Status* and *TXModule Identification Registers* may be read by the computer. The effect of trying to access any other registers/memory area is undefined except that an *Error* bit in the *TXModule Status Register* is set.

The halted card may legally be clocked using the single tick function **only in Test mode—**i.e. with *Test Mode Enable* set.

0	Transmitter Module is accepting external System Clock
1	Transmitter Module is **not** accepting external System Clock

3.3.6.2 Stop

Bit 1

This bit is set by the card when it detects a *STOP* signal from the Timing Control Module. The Timing Control Module generates a *STOP* signal to halt the system. The effect of receiving the *STOP* signal is for the Transmitter Module to ignore further external System Clock pulses, and set the *Card is Halted* and *Stop* bits.

The *Stop* bit remains set until the computer clears it by writing a 1 to *Clear Stop* or to *Global Reset*.

0	No TCM *STOP* pulse since power-up or *Stop* bit last cleared
1	TCM *STOP* pulse has been detected

3.3.6.3 Error
Bit 2

This bit is set by the Transmitter Module when it detects that the computer has tried to perform an illegal operation. The normal result of the operation in undefined. The *Error* bit remains set until the computer clears it by writing a 1 to *Clear Error* bit or the *Global Reset*. The reason for the error bit being set is displayed in the *Error Register*.

0	No error since power-up or this bit cleared
1	Error since last reset or bit cleared

3.3.6.4 Data Valid & Control Valid (CAV/DAV*)* ¥
Bits 3 & 4

These bits are used to indicate the type of information being sent to the output of **both** of the G-links.

Control Valid	*Data Valid*	
0	Don't care	D0-D8 and D9-D15 is being sent as control word information (Control Mode)
1	0	Parallel word data (D0-D15) is being sent as data information (Data Mode)
1	1	Data link is not used so the Data Encoder sends Fill Frames (FF) to maintain the DC balance and allow the receiver to maintain frequency and phase lock (Fill Frame Mode)

When the pipeline is active (i.e. *Card is Halted* = 0), the G-link will be set in Data Mode and when the pipeline is inactive the G-link will be in Fill Frame Mode. Control Mode should not be seen during normal operation.

3.3.6.6 G-link Locked 0,1 ¥
Bit 5

This bit indicates the **lock status** of the G-link phase locked loop for **channels 0 &1**. A set value indicates lock. This signal may give multiple false-lock indications during the acquisition process, so should be debounced if it is used for any other purpose than to drive the Rx G-link chip.

0	G-link transmitter PLL not locked for channels 0 &1
1	G-link transmitter PLL locked for channels 0 &1

3.3.6.6 G-link Locked 2,3 ¥
Bit 6

This bit indicates the **lock status** of the G-link PLL for **channels 2 & 3**. A high value indicates lock. This signal may give multiple false-lock indications during the acquisition process, so should be debounced if it is used for any other purpose than to drive the Rx G-link chip .

0	G-link transmitter PLL not locked for channels 2 & 3
1	G-link transmitter PLL locked for channels 2 & 3

¥Note: When the Daughter Card is absent this bit is undefined.

3.3.7 BCID Xilinx Control Register

Bit	Descriptive Name	Signal name	
0 (LSB)	*Peak Finder Override*	PFOVR	
1	*FIR Filter Enable*	FIREN	
2	*Output Enable*	OUTENB	
2-15	Unused		Always 0 on read

The function of this register is to provide control over the bunch crossing identification algorithm once the Xilinx FPGA has been down-loaded with its configuration. The bits drive I/O pins on the FPGA which have no meaning until it has been configured with a BCID program.

3.3.7.1 Peak Finder Override
Bit 0

Setting this bit asserts the PFOVR line on the Xilinx FPGA. If set, this bit causes the BCID data to be written continuously to the output stream (i.e. Straight-through mode). If clear, the output stream is all zeros except for the single byte representing the peak

0	Data stream **is** fed through the Peak Finder Algorithm
1	Data stream **is not** fed through the Peak Finder Algorithm

3.3.7.2 FIR Filter Enable
Bit 1

Setting this bit asserts the FIREN line on the Xilinx FPGA. If set, this bit causes the output data stream to be taken from the Finite Impulse Response filter instead of from the pipeline.

0	Data stream **is not** fed through the FIR filter
1	Data stream **is** fed through the FIR filter

Usual settings for these bits are as follows:

Peak Finder Override	FIR Filter Enable	Operation
0	0	Normal beam line operation—bunch crossing identification enabled—output on peak only.
1	0	Straight-through mode—FPGA inputs copied to outputs unchanged. Used for testing and debugging.

3.3.7.3 Output Enable
Bit 2

This bit field controls the *OUTENB* pin on the Xilinx, which switches the I/O pins between being tristated and active. For normal Xilinx operation, *Output Enable* must be set to 1. It is provided for possible diagnostic purposes.

3.3.8 BCID Xilinx Program Register

Bit	Descriptive Name	Signal name	
0 (LSB)	*Data*	*DIN*	Reg. Bit
1	*Hold Program*	*HOLD_PROG*	Reg. Bit
2	*Configuration Clock Enable*	*CCLKEN*	Always 0 on read.
3	*Not initialised*	*INIT* (*DAT3P5_7*)	(RO)
4	*Done*	*DONE*	(RO)
5-15	Unused		Always 0 on read

This register is used to program the Xilinx FPGA in slave serial mode. In slave serial mode, the Xilinx monitors a single I/O pin during configuration. The configuration program is sent as a bit stream to this pin and clocked into the Xilinx FPGA by the rising edge of a configuration clock provided as an input to the chip.

The strategy to be adopted here for loading the Xilinx FPGA is:

1. The *Hold Program* and *Configuration Clock Enable* fields are set to zero. Clearing *Hold Program* causes the Xilinx FPGA to clear out any existing program.

2. *Hold Program* is set to 1, which will cause the Xilinx FPGA to stand by to start receiving its new configuration bit stream 5 microseconds later.

3. After a suitable delay, the first bit of the configuration program is written to *Data* and in the same register write operation, the *Configuration Clock Enable* field is also set. This will cause this and subsequent writes to the *BCID Xilinx Program Register* to each generate a configuration clock pulse to the Xilinx.

4. Further bits of the configuration program are written to the *BCID Xilinx Program Register.* A few writes after the configuration program has been loaded, the Xilinx will assert the *Done* bit. Note that there is a delay incorporated into the signal to the Xilinx FPGA configuration clock to ensure that there is not a race between the data bit and the clock edge.

The steps required are summarised by the following table:

Hold Program	*Conf. Clock Enable*	*Data*	Action performed
0	0	X	Clear any existing program
1	0	X	Standby to download new program
			Wait at least 5 microseconds
1	Pulse	1/0	Write each bit of configuration to *Data* until program loaded
1	Pulse	X	Continue writing and check *Done* set. If not set within 10 writes, then the Xilinx FPGA detected an error in the configuration program
1	0	X	Disable configuration clock

3.3.8.1 Data
Bit 0

This bit is connected to the serial data bit stream input on the Xilinx and is used to load the configuration program bit serially.

3.3.8.2 Hold Program
Bit 1

This bit is connected to the <u>*/PROGRAM*</u> signal of the FPGA. When *Hold Program* is cleared (0), the Xilinx FPGA goes into a continuous loop clearing its configuration memory. This causes the FPGA's <u>*DONE*</u> signal to be pulled down and thus the *Done* bit cleared.

When *Hold Program* is subsequently set, the FPGA finishes its current clear cycle and enters a state where it can start loading its configuration memory. This process takes about 5 microseconds, so there must be a delay of a least this period between the *Hold Program* bit being set and the first bit of data to be written to it.

0	Clear Xilinx FPGA configuration program
1	Read in configuration program if not already configured.

3.3.8.3 Configuration Clock Enable (Pluse Bit)
Bit 2

When this bit is set a clock pulse is generated. This bit enables the VME write strobe to be used as the Xilinx FPGA configuration clock when the *BCID Xilinx Configuration Register* is addressed. When set, each time that the computer writes to this register, bit 0 will be strobed into the FPGA.

3.3.8.4 Not Initialised
Bit 3

This is connected to the <u>*/INIT*</u> pin on the FPGA. It is held low whilst the FPGA is undergoing power stabilisation and initial clearing of memory. When the program is being downloaded into the FPGA it is held high. If an error is detected in the program during loading, then it is pulled low.

It is not anticipated that this bit field will be used, but it is available for monitoring by the computer. If this field becomes zero when *Done* is zero then a configuration error has occurred. However, the computer will normally detect this by the *Done* bit not becoming set when it has finished writing the configuration program.

After *Done* becomes set, the value of this bit is undefined. This is because the signal line on the FPGA used for it becomes reallocated as a user-defined I/O line.

To facilitate configuration, the <u>*/INIT*</u> line is weakly pulled high by a pull-up resistor, but this will be overridden when the <u>*/INIT*</u> line is actively driven by the Xilinx FPGA after configuration.

If *Done* is clear (i.e. 0), then the *Not Initialised* bit means:

0	FPGA undergoing power-up initialisation or error has been detected
1	If program being loaded, then no error so far

If *Done* is set (i.e. 1), then the *Not Initialised* bit means:

0 or 1	No interpretation possible. */INIT* is reallocated as an I/O pin (and thus this bit shows the value of the I/O pin).

3.3.8.3 Done
Bit 3

This bit is set when the FPGA contains a valid configuration program. It is driven by the FPGA's *DONE* signal.

0	FPGA not loaded
1	FPGA is loaded with a valid configuration program

3.3.9 G-Link Control Register ¥

Bit	Descriptive Name	Signal name	
0 (LSB)	*Div0*	*DIV0*	
1	*Div1*	*DIV1*	
2-3	Unused		Always 0 on read
4	*G-link Reset 0,1*	GRST01	Always 0 on read
5	*G-link Reset 2,3*	GRST23	Always 0 on read
6-15	Unused		Always 0 on read

¥Note: When the Daughter Card is absent these bits have no effect.

3.3.9.1 Div0/Div1 ¥
Bits 0 & 1

These bits determine the baud rate of the outputs of both G-Links.

DIV1	*DIV0*	Serial Baud Rate (MBaud) Range	
		Minimum	Maximum
0	0	840	1500
0	1	420	1010
1	0	210	505
1	1	150	253

The baud rate will normally be set at 800 MBaud, this will put it in the range of 420—1010 MBaud. Thus, the usual setting should be *Div0* = 0 and *Div1* = 1.

3.3.9.2 G-link Reset 0,1 ¥

Bit 4 Input to card

When *GRST01* is set, the internal registers of the G-link chip driving channels 0 & 1 are reset.

0	Read value, no effect on writing
1	Resets the internal registers in G-link 0 (by generating a pulse).

3.3.9.3 G-link Reset 2,3 ¥

Bit 5 Input to card

When *GRST23* is set, the internal registers of the G-link chip driving channels 2 & 3 are reset.

0	Read value, no effect on writing
1	Resets the internal registers in G-Link 1

3.3.10 Scrolling Memory Counter Register ¥

This read-only register contains the last value of the 8-bit scrolling memory counter which was used to address the input, output and (in Test mode) lookup table memories. Each clock pulse—either a tick or system clock—causes the counter to increment **after** the memories are accessed. It rolls through FF to 00.

The address range is 256 bytes for each memory. However the input and output memories appear to be duplicated in VME address space—each memory location has two addresses separated by 256. This simplifies access by the computer when reading data which spans the end and beginning of the memory. It simply begins the read towards the end of the first address range and finishes in the second.

The computer can only access *Counter Register* when the pipeline is inactive (i.e. *Card Is Halted* is set).

The latched value of a physical counter on the module is used to address the memories, and it is this latched value which the computer reads. Thus, the interpretation of the value is the **last memory address accessed by the module before it was halted**. This means that if the physical counter is cleared (by *Scrolling Memory Counter Reset*), the latched value will not until it is latched through from the counter just prior to the next memory access.

Bits	Meaning
0-7	Latched counter value used for last memory access
8-15	Always 0 on read

3.3.11 Error Register

This read-only register contains a non-zero value when the *Error* bit in the *TXModuleSR* is set. The value is interpreted as a bit mask which indicates the reason or reasons for the error. It is cleared by all circumstances which clear the *Error* bit.

Three bits are defined, corresponding to these reasons:

Bit	Meaning
0	Attempt to generate single tick when the module was not halted
1	Attempt to access an unused VME address in the card's address space
2	Attempt to access register or memory other than *TXModule Identification*, *TXModule Control* or *TXModule Status Registers* when the module was not halted
3-15	Unused - Always 0 on read

3.3.12 Finisar Diagnostic Register

The Finisar has bit serial interfaces for setting and reading various diagnostic information. Because this is a relatively unimportant function for the Transmitter Module, convenience has been sacrificed to ensure adequate board space to implement other functions.

Bit	Descriptive Name	Signal Name	
0	*Serial Out*	*FTM_SO*	Read only
1	*Serial In*	*FTM_SI*	
2	*Serial Clock*	*FTM_SCLK*	
3	*Ready*	*FTM_RDY*	Read only
4	*Chip Select*	*FTM_CS*	
5	*Finisar Select*	*FINSEL*	
6	*Diagnostic Reset*	*FTM_RST**	Always 0 on read
7-15	Unused		Always 0 on read

Byte length commands and responses are clocked through the *Serial Out* and *Serial In* bit fields on the falling and rising edge of *Serial Clock* respectively. The response to a command (such as a value when the command is to read the value) is clocked out of the device as the **next** command is clocked in.

Probably the best way of reading a single value is therefore to issue the command to read the value twice, as the response from the first command will be clocked out whilst the second duplicate command is being clocked in.

As there are two Finisar devices, *Finisar Select* is used to select which one the signals in the rest of the register refer to. The Finisar device diagnostics are driven in the following fashion:

SO	*SI*	*SC*	*Rdy*	*!CS*	*FS*	Action being performed
	X	0		1	1/0	Select desired Finisar FTM-8510-1, and assert its chip select
						Wait at least 1 ms, then ensure that *Ready* is 1
	1/0	0		1	"	Load first bit of command into *Serial In*
"	"	1		1	"	Set serial clock edge high to shift bit in.
"	"	0		1	"	Set serial clock edge low again. This will shift response of last command into *Serial Out*, but we probably want response from this command!
"	"	1/0				Repeat above two steps 7 more times. Command has now been shifted into Finisar
						Repeat previous 3 steps. This will re-issue the command but also shift out the results of the first time the command was executed. Read out each bit in turn from the *Serial Out* immediately after each clear of *Serial Clock*

¥Note: When the Daughter Card is absent this register will have no effect.

3.3.12.1 Serial Out
Bit 0

This read-only field contains buffered bit serial data as shifted out of the Finisar on falling edges of the serial clock.

3.3.12.2 Serial In
Bit 1

This field is for data which is to be bit-serially shifted into the Finisar diagnostic port on rising edges of the serial clock.

3.3.12.3 Serial Clock
Bit 2

This field is connected to a latch which drives the serial clock used to shift data in and out of the Finisar. Thus the device is clocked by alternately writing 0 and 1 to this field with other fields in the register remaining the same.

3.3.12.4 Ready
Bit 3

This is a buffered output from the Finisar device, and indicates that the Finisar is ready to accept commands. It becomes set no more than 1 ms after the chip select <u>/CS</u> signal has been asserted.

3.3.12.5 Chip Select
Bit 4

This bit-field is used in conjunction with the *Finisar Select* to select device for diagnostics. *Chip Select* is inverted and used to drive the /CS line on the selected Finisar device. After setting this bit, the computer should wait at least 10 ms and then verify that the *Ready* field has become set before issuing diagnostic commands. If *Ready* does not become set, then this probably indicates a hardware fault.

0	Finisar not selected (i.e. /CS is high)
1	Finisar selected (i.e. /CS is low)

3.3.12.6 Finisar Select
Bit 5

This field controls the destination for the output from the *Chip Select* bit, and thus which Finisar can be enabled for diagnostics. The Finisar which is not selected has its /CS pulled high so is deselected. With the exception of the /CS, corresponding input and output **diagnostic** pins on both Finisars are connected to the *Finisar Diagnostic Register*.

Contention is avoided because one of the Finisar device will be deselected by the setting of *Finisar Select*, and will thus tristate its pins.

Thus, the settings of the two bit-fields have the following meaning:

Chip Select	*Finisar Select*	Effect
0	0	No Finisar selected for diagnostics
0	1	No Finisar selected for diagnostics
1	0	Finisar 0 is selected
1	1	Finisar 1 is selected

3.3.12.7 Diagnostic Reset
Bit 6

Setting this bit will reset the diagnostics in the selected Finisar. This may be useful if it is thought that the Finisar diagnostics is in an unknown state, for example if the number of clock pulses issued so far to clock data in and out is unknown. It is prudent to assert it each time that a Finisar is selected.

3.3.13 DELAY01 & DELAY23 Registers ¥

These registers control the delay between the output from the FPGA and the input to the G-link. There are two registers; DELAY01 controls coarse delay for BOTH pairs of channels and the fine delay for channels 0 & 1; DELAY23 controls the fine delay for just channels 2 & 3, this register does not effect the coarse delay.

There are restrictions on the values which can be specified because the delays are implemented using FIFOs whose depth is specified by the coarse delay, whilst the fine delay specifies the interval between writing and reading clocks of the FIFO.

The restrictions are:

- The minimum coarse delay is one clock period, a value of zero should not be specified.

- The maximum fine delay should not be specified as more than one clock period.

DELAY01

Register Bits	Assignment	Description
0-4	DelA[0:4]	1 ns steps for **Fine timing delay** with a max. range of one system clock period.
5-7	Unused	Always 0 on read
8-12	DelB[0:4]	**Coarse timing delay** in steps of the system clock period, 25 ns steps at a system clock of 40 MHz. Minimum legal value is 1.
13-15	Unused	Always 0 on read

DELAY23

Register Bits	Assignment	Description
0-4	DelA[0:4]	1 ns steps for **Fine timing delay** with a max. range of one system clock period.
5-15	Unused	Always 0 on read

¥Note: When the Daughter Card is absent the low bytes of both delay registers are undefined.

3.3.14 Daughter Module ID Register

This is a read-only register which contains the serial number of the daughter board. If no daughter board is fitted, then the serial number will be read as zero (this will only be true when intially tesing the Mother Board. Otherwise, daughter board serial numbers will start at 1. Note that the Finisars and G-links will be fitted to the Daughter Card.

In this case, attempts to access registers pertaining to absent components will produce unpredictable values, but will not cause VME bus time-outs.

3.3.15 IPMem and OPMem

The Input and Output Monitoring Memories are used when the pipeline is active to spy upon the data in the pipeline. These memories will be 256 bytes per channel and constantly scrolling (barrel store memories). They will monitor the data at the input just after the input latches and at the output just after the Xilinx FPGA.

Memory location bits for a time slice	Input RAMs	Output RAMs	Memory for channel
0-7	Input RAM 3	Output RAM 3	Channel 3
8-15	Input RAM 2	Output RAM 2	Channel 2
16-23	Input RAM 1	Output RAM 1	Channel 1
24-31	Input RAM 0	Output RAM 0	Channel 0

Input RAM records the input FADC data.

Output RAM records the data after the BCID algorithm logic implemented in the FPGA has been applied but before the conversion for serial transmission.

Each of the 4 channels has an 8-bit input and output monitoring memory, these are to be paralleled into a 32-bit Long word that represents the 4 channel for a given time slice. If the data is interpreted as bytes, the data shall be provided for each time slice and fed in order to bytes 0, 1, 2 & 3 of each 32-bit word.

Read Block Transfers (BLT) from the Input and Output monitoring memories are allowed. The base address is latched in an 8-bit counter and then incremented on each read access of the block transfer. If the block transfer crosses a memory block boundary of 256 then the counter will roll round to the beginning of the memory block of 256.

The memory space for the Input and Output monitoring memories is doubled up to aid rapid reading. This uses the same physical memory device but doubles the address space. This is done by ignoring the 9^{th} bit A8 in the decoding of the address lines.

3.3.16 Lookup table (LUT) Memories 0-3

The lookup table (LUT) memories are part of the data pipeline. Raw data entering the board is used as the address in the lookup table memory and the data stored at the corresponding memory location is then piped to the FPGA.

The lookup table memories can also be used in a Test mode in which they are loaded with test vectors, and then scrolled through using the scrolling memory counter. These vectors will then be piped to the FPGA in order of ascending addresses.

The memories form a contiguous block, with the first 256 words addressing the lookup table memory for channel 0. The memory for each channel is only 256 bytes long, so words in VME address space are mapped onto bytes in the memories. This means that when writing, the upper byte of each word is ignored. Similarly, the upper byte of each word always contains zero when memory addresses are read.

3.4 Manufacturing

The manufacture of the PCBs will be carried out by an outside manufacturer in two stages, first stage: Mother Board and second stage: Daughter Card. It is estimated that both PCBs will be an 8-10 layer board. The assembly will be done externally.

3.5 Testing and product control

3.5.1 Strategy

There will be two stages of testing:

1) Stand-Alone: This is when the Transmitter Module can be proved to work, using the already proven Analogue to Digital Modules and a test card for example. The Mother Board will be commissioned first followed by the Daughter Card.

2) In-System: This is when the Transmitter Module will be proved to work in the system with the ADM, CPM and TCM.

The lookup table memories can be utilised to inject test vectors into the data pipeline. A receiver test card will be required to capture the transmitted optical and electrical signals. This will require a Finisar receiver (FRM-8510) and a G-link receiver (HDMP-1014).

A signal generator will be used to inject signals into the ADM which inputs data onto the front of the Transmitter Module.

3.5.2 Software

Test software will be required from the customer . The functions that are required to be tested are:-

- Low level (i.e. memory access)
- Pedestal subtraction and calibration
- Bunch Crossing Identification (BCID)
- Serialisation
- Transmission optically
- Transmission electrically

These functions need to be tested in both Stand-Alone and In-System testing stages.

The software will use the VME D32:D16 bus interface to communicate with the Transmitter Module.

3.6 Installation

The Transmitter Module is designed to sit in a 6U crate with a VME (J1, J2) back plane. The module will be provided with a front panel containing sockets and monitoring LEDs.

3.7 Maintenance and further orders

This is a demonstration module with an expected life span of no more than two years, hence there in no long term maintenance requirement. Three Transmitter Modules will be required for this phase of the demonstration program:
1) Two for CERN
2) One for the UK
An approximate total of twelve (3 now and 9 later) Transmitter Modules for the next demonstration phase.

4. Project Management

4.1 Personnel

		RAL Ext.	RAL Location
Customer:	A.R.Gillman	5521	R1, 1.54
Project Manager:	V.Perera	5692	R68, 2.31
Software Engineer:	J.Leake	6803	R1, 1.30
Project Engineer:	G.C.Lewis	5308	R25A, 84

4.2 Deliverables

To the Customer: Three Transmitter Modules and one test card.

From the Customer: Test Software, Powered VME crate (with J1 and J2 connectors) and a software platform to allow the test software to drive the Transmitter Module.

4.3 Project plan

No.	Task break down:	Planned Completion Date	Actual Completion Date
1	Produce a specification (QA).		11 AUG 95
2	Functional TXM Design .		10 NOV 95
3	Fitting TXM Design (physical Space).		12 JAN 96
4	Tracking Layout TXM (Mother).		7 FEB 96
5	Layout TXM (Daughter)	16 FEB 96	
6	PCB assembly (Mother).	4 MAR 96	
7	PCB assembly (Daugnter).	13 MAR 96	
8	Test (TXModule 1) (4 wks)	1 APR 96	
9	Test (TXModule 2) (2 wks)	15 APR 96	
10	Test (TXModule 3) (2 wks)	29 APR 96	

4.4 Design Reviews

Milestone	Planned Date	Actual Date
PDR		10 AUG 95
IDR (TXM card designed)		3 NOV, 10 NOV 95
FDR (Mother Board)		8 FEB 96
FDR (Daughter Board)	16 FEB 96	
TXM assembly (Mother)	4 MAR 96	
TXM assembly (Daughter)	13 MAR 96	
TXM operational one TXModule tested	1 APR 96	
All three TXM units operational	29 APR 96	

4.5 Training

Training will be carried out as required on the job in the use of Cadnetix, Xilinx, PLD and ABEL.

4.6 CAE and test equipment

CAE: Cadnetix for schematic capture, FPGA programming language for control logic (ABEL 6) and FPGA configuration.

Test equipment:
(1) VME crate
(2) VME card to act as master
(3) Computer to run software
(4) Receiver test card (£1500)
(5) Logic analyser
(6) Oscilloscope
(7) Function generator
(8) System Modules :- ADM, CPM, TCM
(9) VIC
(10) Two VME Extenders

4.7 Costs and finance

Cost centre: FK400PP

Quote	**Mother**		Total
	Non Recurrent Cost	Recurrent Cost	
Production unit cost		£370 ea.x3	£1,110
Tooling & Netlist Test	£525		£525
Bare Board Cost			£1,635
Assembly Tooling	£150 per side x 2		£300
Assembly placement		£150 x 3	£450
Assembly Cost			£750
3 Mother Boards			£2,385

Estimate	**Daughter**		Total
	Non Recurrent Cost	Recurrent Cost	
Production unit cost		£300 ea.x3	£900
Tooling & Netlist Test	£500		£500
Bare Board Cost			£1,400
Assembly Tooling	£200 per side x 1		£200
Assembly placement		£150 x 3	£450
Assembly Cost			£650
3 Daughter Cards			£2,050

	Non Recurrent Cost	Recurrent Cost	Totals
Mother Board	£825	£1,560	£2,385
Daughter Card	£700	£1,350	£2,050
Front Panel			£50
Components		£1,400 ea.x3	£4,200
Total Ex VAT	£1,525	£7,110	£8,685
Cost per TXM unit Ex. VAT		£2,370	
VAT @ 17.5%			£1,520
Total cost approx.			£10,205

4.8 Intellectual Property Rights (IPR) and Confidentiality

Electronics Division owns the layout and schematic databases. Any masks or phototools will be procured by the Division. None of these items will be released outside the agreed ATLAS collaborators unless the appropriate protective agreements are in place.

4.9 Safety

General laboratory safety codes apply. A class 1 laser is used in this module and hence it may be required to carry appropriate warnings.

4.10 Environmental impact

RAL will dispose of the modules at end of their life.