Update on energy summation algorithms

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  - DAQ read-out path
  - Control path
- Jet-/EnergySum FPGA
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  - Control path
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Overview

Target technology:

- InputFPGA: Xilinx Spartan 2 (XC2S 150 –5 FG 456 C)
- Jet/Energy-Sum Processor: Xilinx Virtex E (XCV 600E –7 FG 680 C)
  (will change due to the need for more logic resources to host
  both jet and summation algorithms)

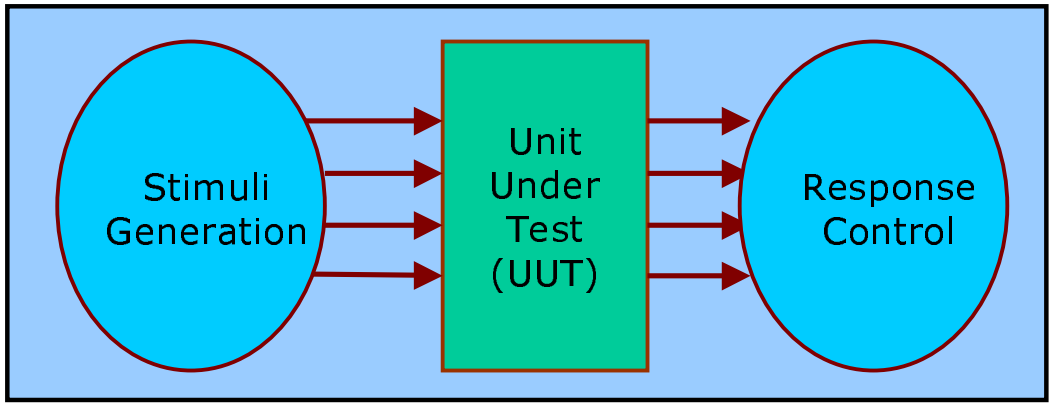
Software:

- Design entry: Renoir 2000.2
- Synthesis: Leonardo 2000.1a2
- Simulation: ModelSim 5.4d

} Mentor Graphics FPGA Advantage

- Place & Route: Xilinx Foundation 3.2i

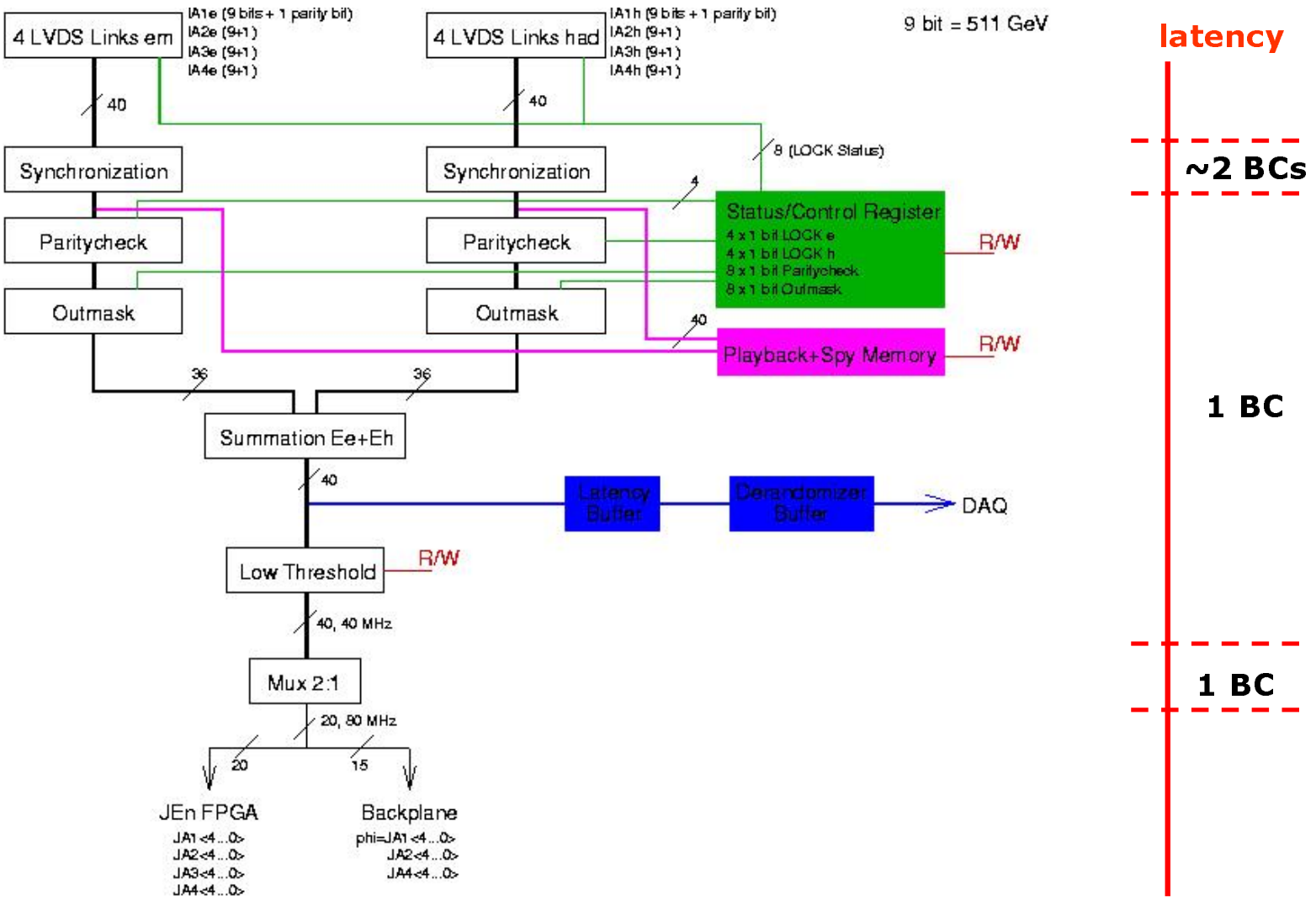
Testbench



Testbench strategy:

- Use testbench with one VHDL-model (UUT is instantiated, stimuli generation and response control are both part of the testbench)
- Testbench is mainly used for simulation (RTL, Gate-level with/without timing) of real-time data path and DAQ read-out path
- Random number generator is used to provide test words for input data
- Testvectors can be interfaced to testbench as ASCII files

Input FPGA


4 LVDS Links em
IA1e (9 bits + 1 parity bit)
IA2e (9+1)
IA3e (9+1)
IA4e (9+1)
4 LVDS Links had
IA1h (9 bits + 1 parity bit)
IA2h (9+1)
IA3h (9+1)
IA4h (9+1)
9 bit = 511 GeV
40
40
8 (LOCK Status)
Synchronization
Synchronization
4
Status/Control Register
4 x 1 bit LOCK e
4 x 1 bit LOCK h
8 x 1 bit Paritycheck
8 x 1 bit Outmask
R/W
Paritycheck
Paritycheck
Outmask
Outmask
40
Playback+Spy Memory
R/W
36
36
Summation Ee+Eh
40
Latency Buffer
Derandomizer Buffer
DAQ
Low Threshold
R/W
40, 40 MHz
Mux 2:1
20, 80 MHz
20
15
JEn FPGA
JA1<4...0>
JA2<4...0>
JA3<4...0>
JA4<4...0>
Backplane
phi=JA1<4...0>
JA2<4...0>
JA4<4...0>
latency
~2 BCs
1 BC
1 BC

Status of InputFPGA

Real-time data path:

- ϕ summation is done in main processor in order to handle FCAL data correctly (see Uli's talk)
- Timing simulation of routed design with testbench shows:
  - algorithm is working up to 50 MHz with chosen device
  - latency is 4 BCs (see Uli's talk for latency issues of JEP)
  - number of slices: 6 %
- Synchronisation is most likely to be adapted from Serialiser FPGA

DAQ read-out path:

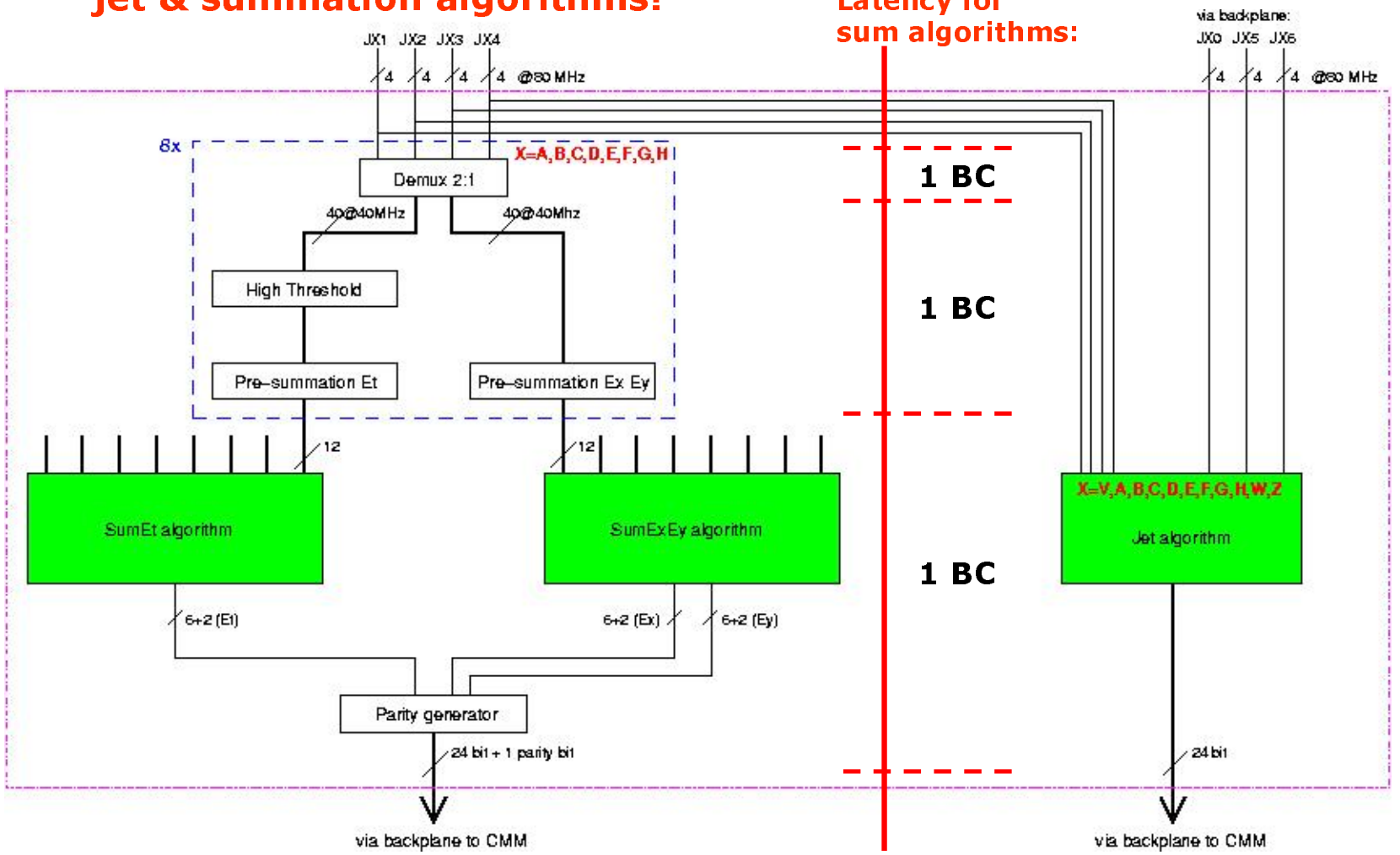
- DAQ read-out path has been implemented and tested in gate simulation:
  - latency buffer is implemented using shift registers
  - derandomizer buffer is implemented using Dual-Port Block SelectRAM Memory (used BlockRAM: 50 %)
  - algorithm is working up to 104 MHz
  - number of slices: 11 %

Control path:

- Provisional memory map has been developed similar to CPM
- Playback + Spy Memory? (depends on available logic resources)

Jet-/EnergySum FPGA

NEW: only one FPGA for jet & summation algorithms!



Not shown: DAQ, Read-out & Control

Status of Jet-/EnergySum FPGA

Real-time data path:

- RTL simulation of E_t algorithm has been carried out
- Gate-level simulation of E_x,E_y algorithm has been carried out
- *Preliminary* design summary after place and route:

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•Device utilization summary:
  Number of External GCLKIOBs          1 out of 4      25%
  Number of External IOBs            197 out of 512    38%
  Number of SLICEs                  1511 out of 6912   21%
  Number of DLLs                       1 out of 8      12%
  Number of GCLKs                      2 out of 4      50%

•Design statistics:
  Minimum period:  24.395ns (Maximum frequency:  40.992MHz)
```

➔ algorithm is working up to 41 MHz with chosen device (see Uli's talk for latency issues of JEP)

DAQ read-out path:

- DAQ read-out path will be adapted from InputFPGA

Outlook

To be done:

InputFPGA:

- Implementation of FCAL data handling
- Timing simulation of DAQ read-out path
- Control path

Jet-/EnergySum processor:

- Implementation of FCAL data handling(➔additional latency)
- Timing simulation of real-time data path
- Adapt tested DAQ path from InputFPGA
- Control path
- Write top level code for jet and summation algorithms
- Conversion in E_x and E_y possible in BlockRAMs (@ 80 MHz) instead of LUT-based multipliers? (➔could save latency!)