Testing the ATLAS Serialiser and CP Chip

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Test Objectives

Serialiser and CP-chip are both FPGA-based designs targeted towards Virtex-E devices.

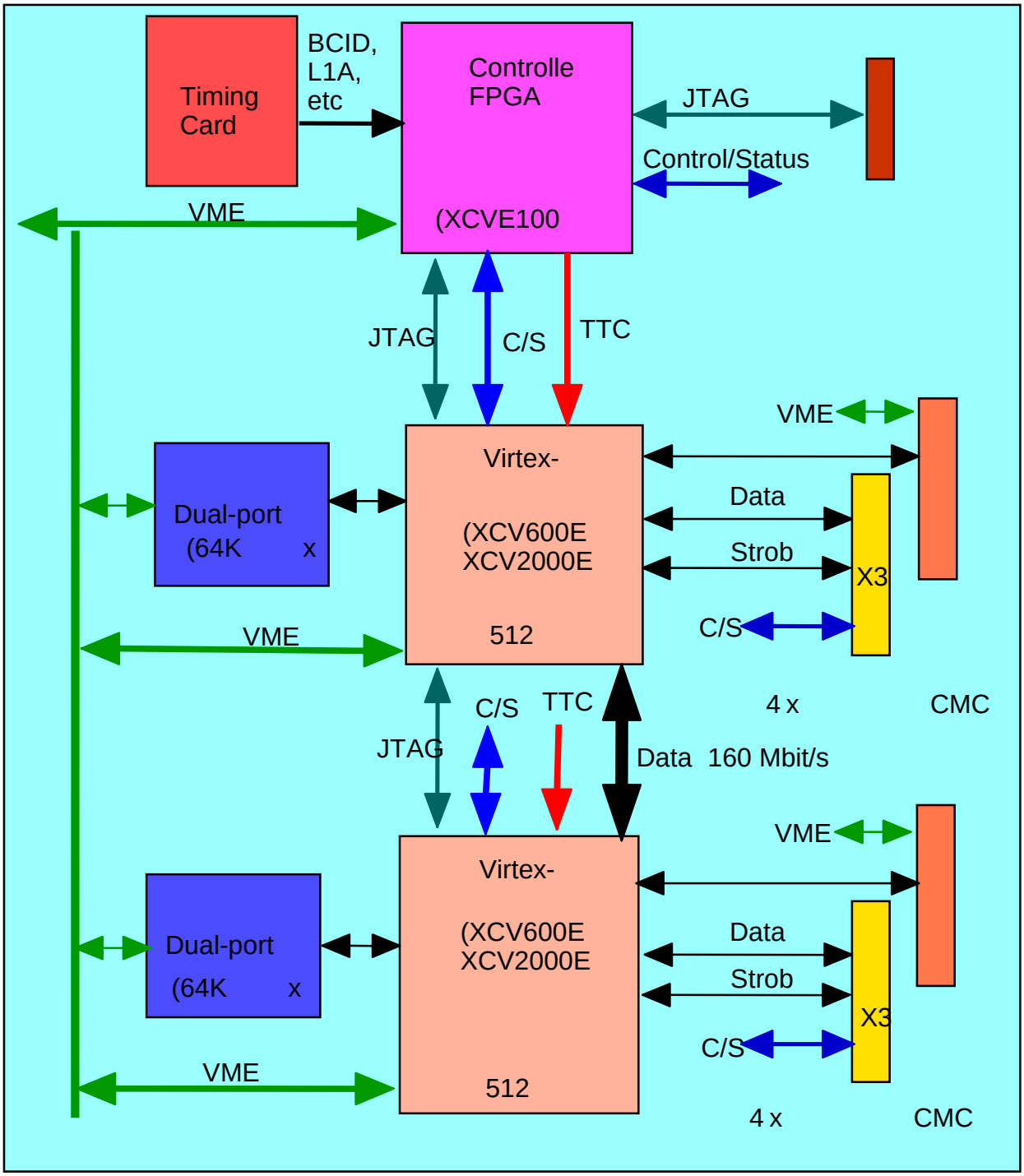
Devices to be used for testing are different from those proposed for final system but of the same family.

Test objectives are to —

- **gain experience working with Virtex-E devices, particularly**
  - **working with large devices (XCV1600E-FG680);**
  - **clocking Virtex-E at 160 MHz.**
- **investigate how hardware performance of designs compares to timing simulation;**
- **demonstrate in hardware that we have working designs for the Serialiser and CH chip.**

Generic Test Module

Simplified block diagram

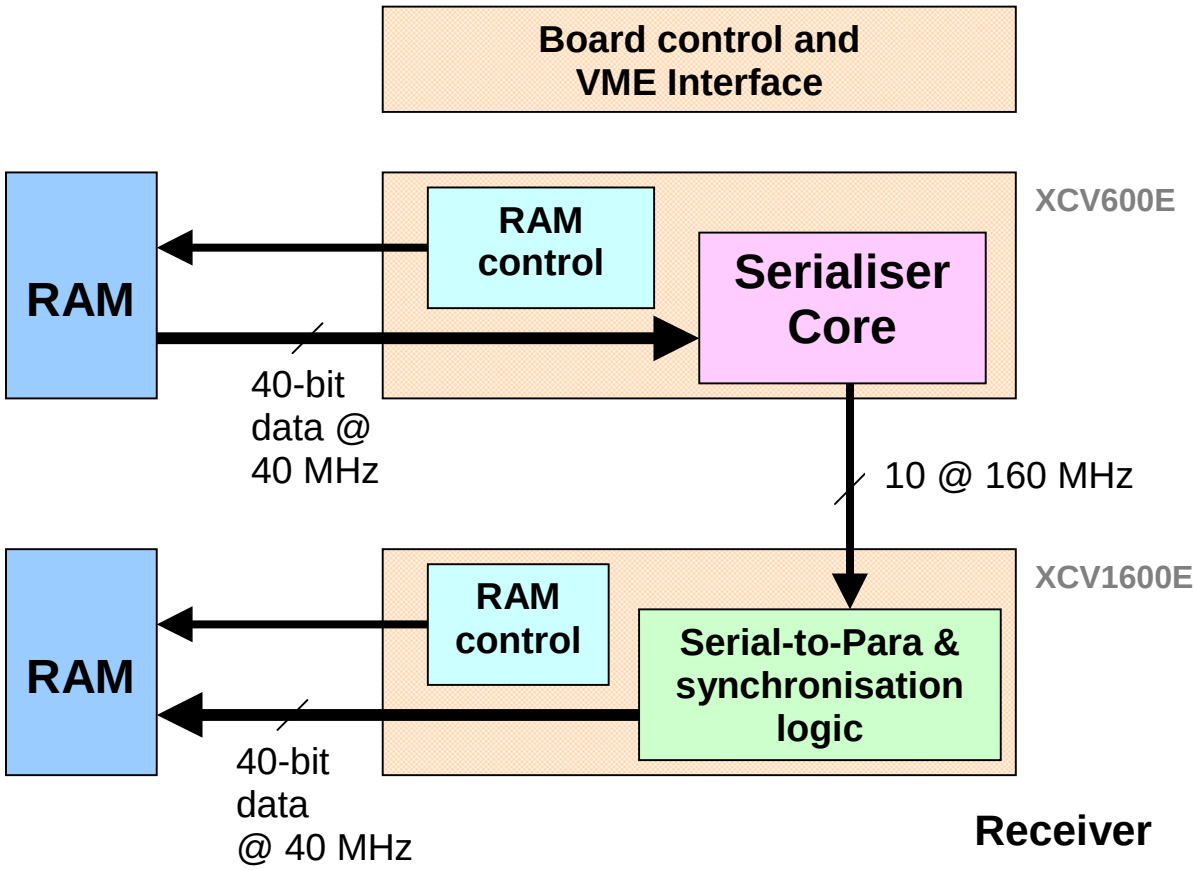


Generic Test Module

- Generic platform for testing FPGA-based designs.
- Design allows for two processor FPGAs in range XCV600E–XCV2000E with FG680 packages
  (fine-pitch ball-grid array with 512 I/O).
- Atlas trigger implementation of board:
  - XCV600E (~900k gates) &
  - XCV1600E (~2M gates)
- Data can be transmitted to and from GTM via (CMC) daughter boards, or sourced and captured locally by dual-port RAMs.
- Timing and trigger control provided by TTCrx test board.
- Specification:

  `http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html`

Testing the Serialiser



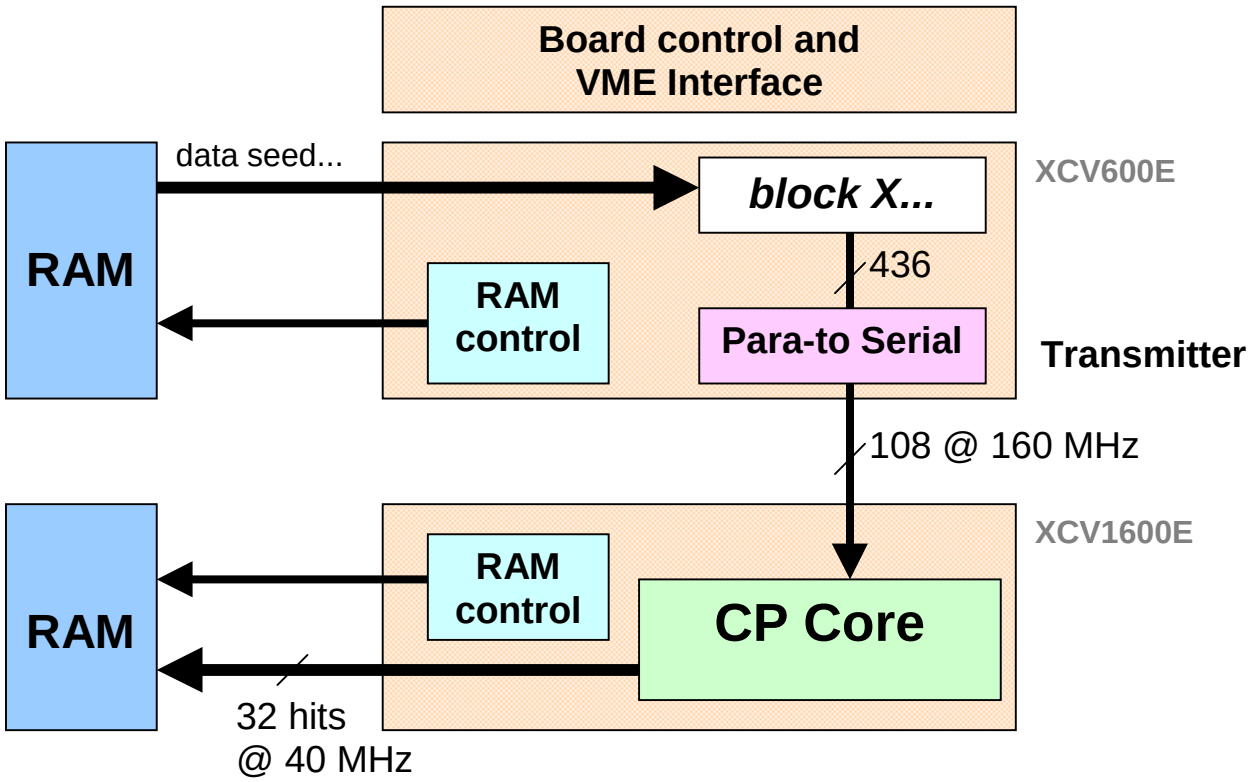
Test Real-time data path; serial-to-parallel conversion @ 160 MHz, Xilinx DLLs.

Serialiser test configuration: existing Serialiser core with added logic to control RAM.

Receiver: Serial-to-Para and sync. logic built from components of CP front end.

Board control and VME decoding: modify existing logic designed by Azmat.

Testing the CP chip



Test real-time data path; synchronising logic, CP algorithm

3 FPGAs to design:

Board control and VME decoding: modify existing logic designed by Azmat.

CP test configuration: existing CP core with added logic to control RAM.

Transmitter: Serial-to-Para and sync. logic built from components of CP front end.

Status

Generic Test Module

Board sent to manufactures 20 Oct... some problems... expected end of November.

Serialiser Test bench

Firmware completed for test implementation of Serialiser and Receiver FPGAs.

VME interface FPGA to be modified as necessary.

CP test bench

To be done.

All firmware should be available for use by the end of November.