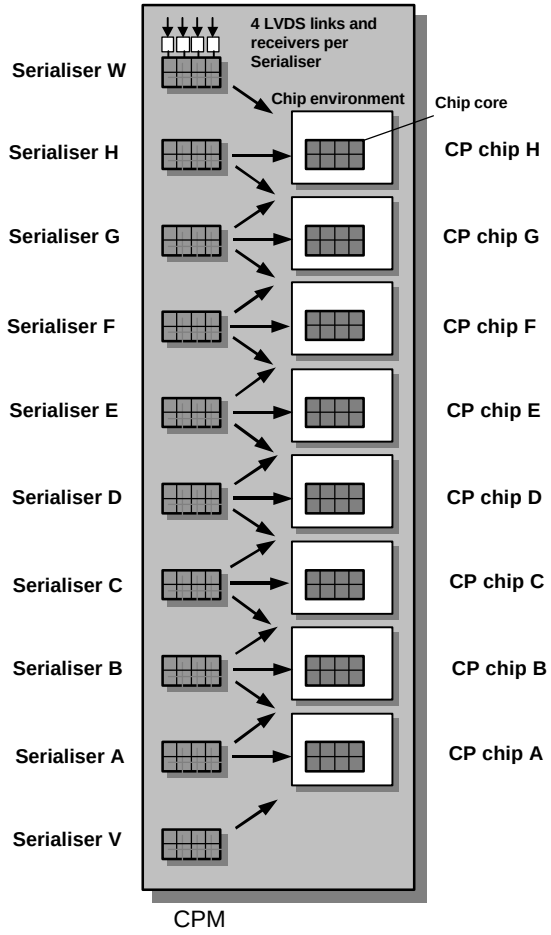
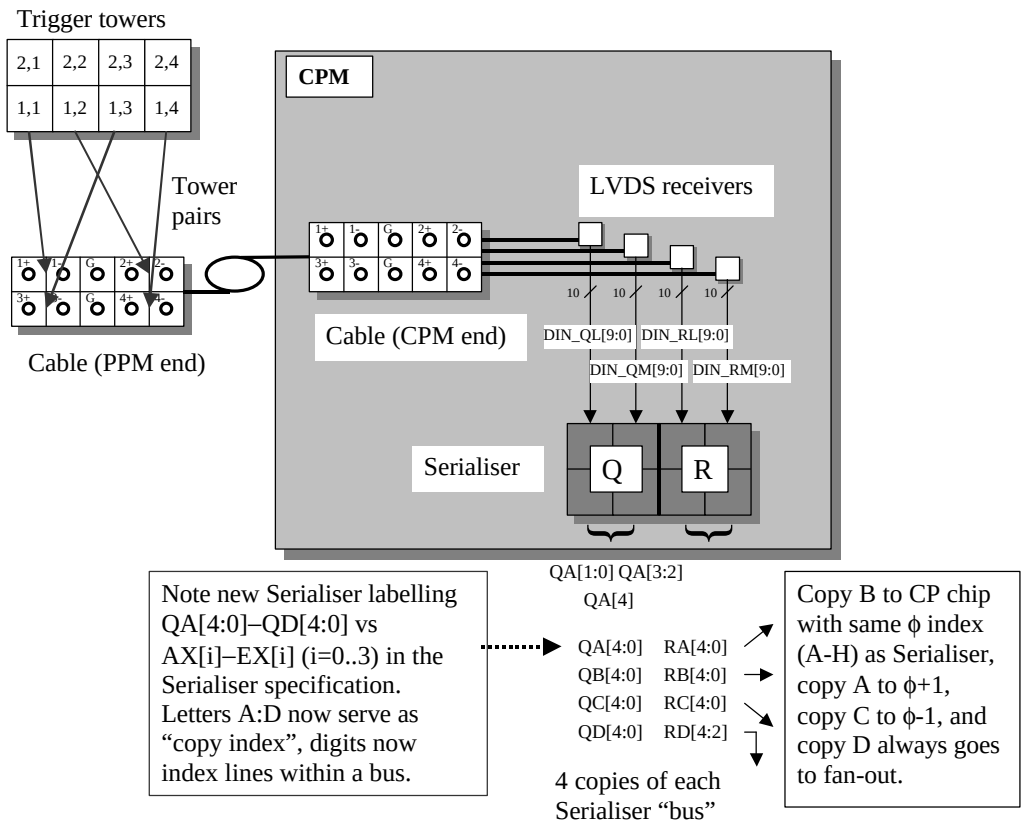
CPM Organisation and labelling

- Mappings between devices
- Labels for CPM signals and CP chip pins
- Some (obvious) CP chip pin assignments



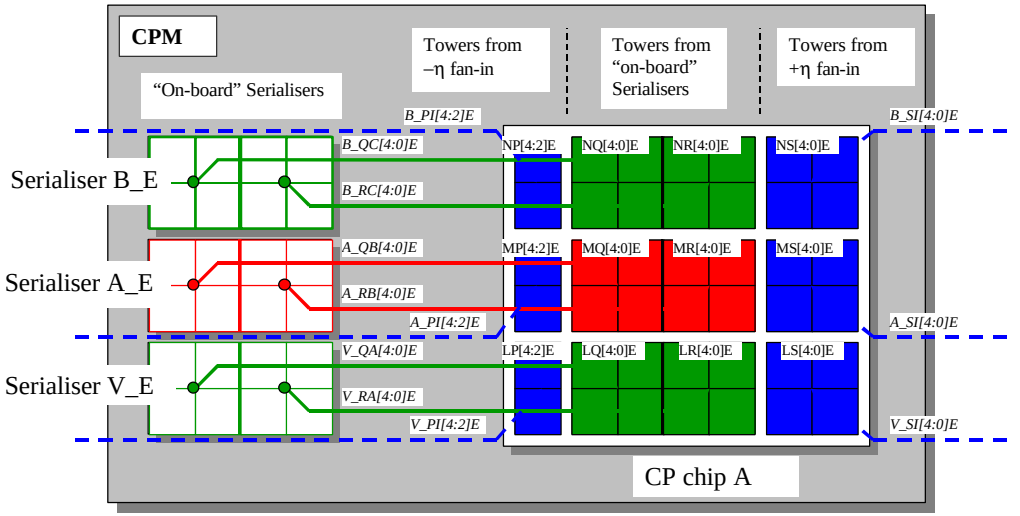
Serialiser I/O

- Assign tower pairs to cables and Serialiser inputs
- 2 tower pairs = ½ Serialiser
- Change Serialiser labelling: halves X & Y => Q & R
- Serialiser output bus QA[4:0]
- Line [4] = flag+parity x2
- Each bus has 4 copies: QA-QC for on-board CP chips, QD for BP fan-out



CP chip signals and pins

- Label CP chip pins and signals
- Inputs from 6 Serialisers,
  plus -/+η fan-in
- Label pins by blocks according to source Serialiser
- L(ower), M(iddle), N(orthern)
- P (-η), Q & R (left/right), S (+η)
- Bus lines labelled [4:0]
- Append E or H for em/had
- Tower signal labels:
  ϕ index + P/Q/R/S + copy A-C (I)
- No labels for backplane signals



NB. Signal labels (italics) and pin labels (roman) shown for electromagnetic data only, indicated by appended "E". All labels re-used for hadronic data with appended "H".

CP chip pin labels (em only shown)

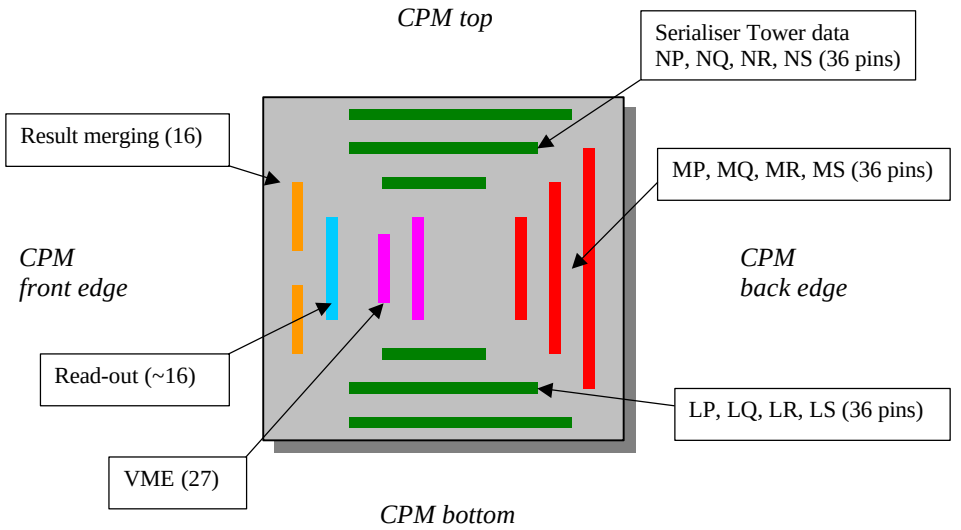
NP[4:2]E NQ[4:0]E NR[4:0]E NS[4:0]E

MP[4:2]E MQ[4:0]E MR[4:0]E MS[4:0]E

LP[4:2]E LQ[4:0]E LR[4:0]E LS[4:0]E

CP chip pin-out

- Given a choice … inputs one side, outputs opposite
- 108 inputs vs 32 outputs (real-time only)
- Put inputs closest to source Serialiser !!!
- Keep read-out signals together (from ROC)



Suggested CP chip pin-out

CPM specification update

- PDR 23rd June 2000: comments and a few design issues
- TTC broadcast implemented in VME Controller
- Read-out simplified, routed through Read-out Controllers
- Latency and power estimates (5V supply and DC-DC conversion)
- FPGA configuration from flash memories (not EEPROMs)
- Two configurations for Serialiser and CP chip (not three)
- Real-time error-counting defined
- Signal labelling defined
- Programming model refined (but still approximate)