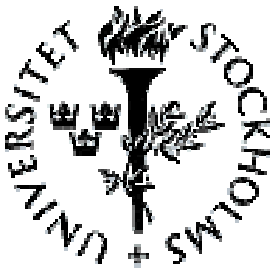


The JEP/CP backplane

Sam Silverstein, Stockholm University

- Processor Backplane specification
- Mechanics demonstrator
- Schedule and milestones

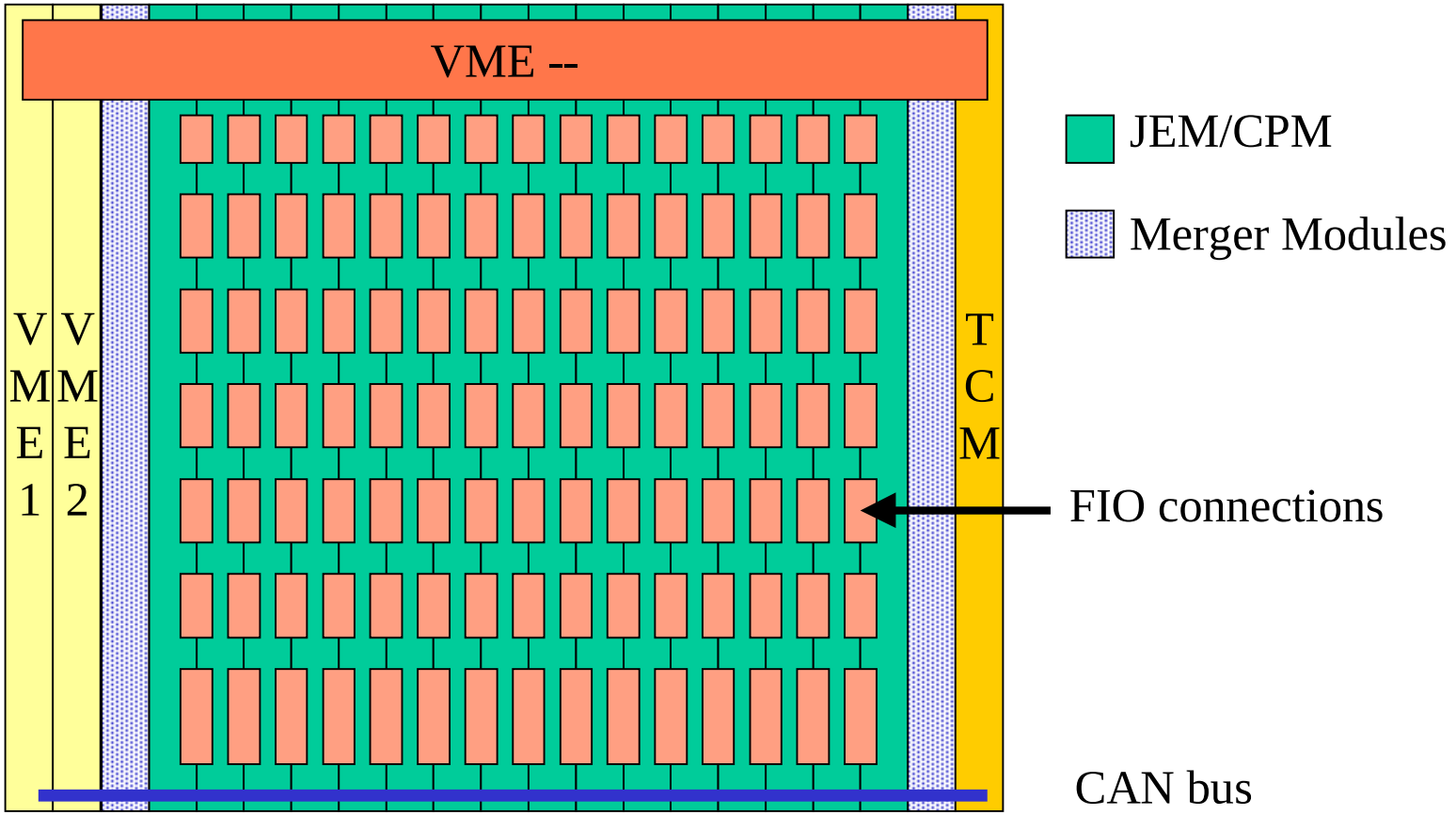
The backplane specification is mature, but not finished

- PDR document version 0.4 on web
  - http://www.physto.se/~silver/trigger/backplanePDR/
  - New draft to be released soon, pending changes at brainstorming session
- Most of document well-reviewed
- Exceptions are:
  - CMM, some VME issues

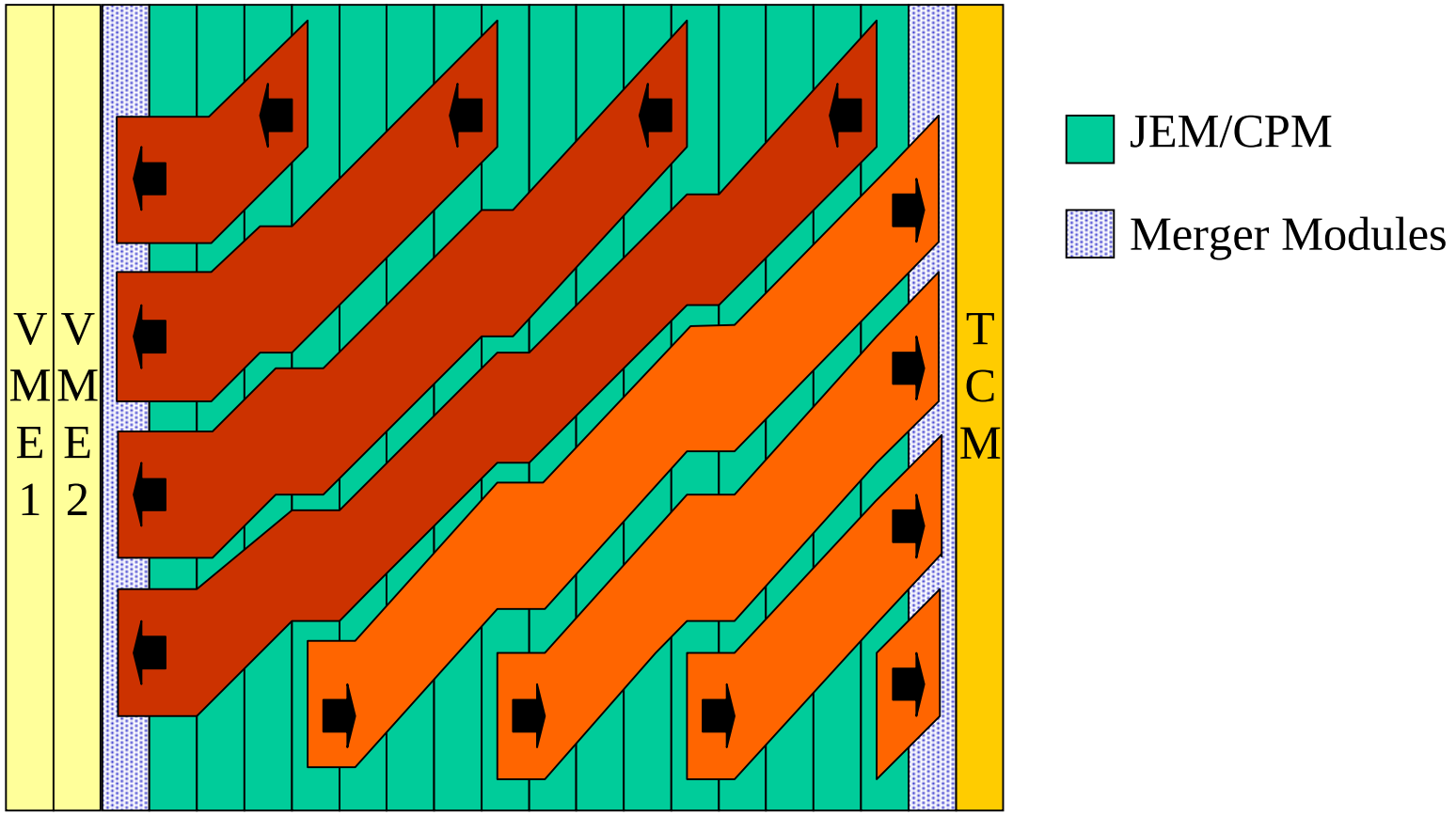
Some backplane numbers

- Approximate dimensions: 395 x 430 mm
- 8 signal and 7 ground layers (15 total)
- Around 23 300 holes, 6 diameters
- 152 connectors, many with shrouds in back of plane
- No power, internal vias, or active components on backplane

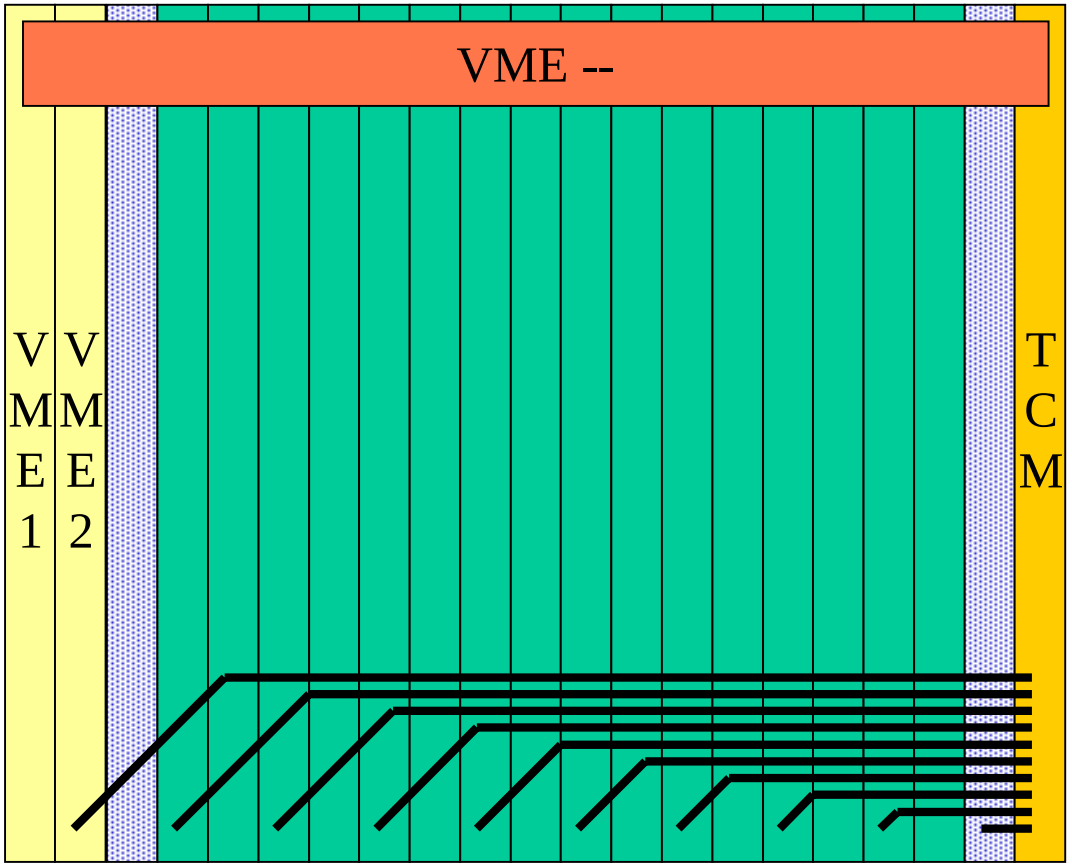
FIO layer (1 of 2)



Merger layer (1 of 4)



”Outer” layer (1 of 2)



JEM/CPM

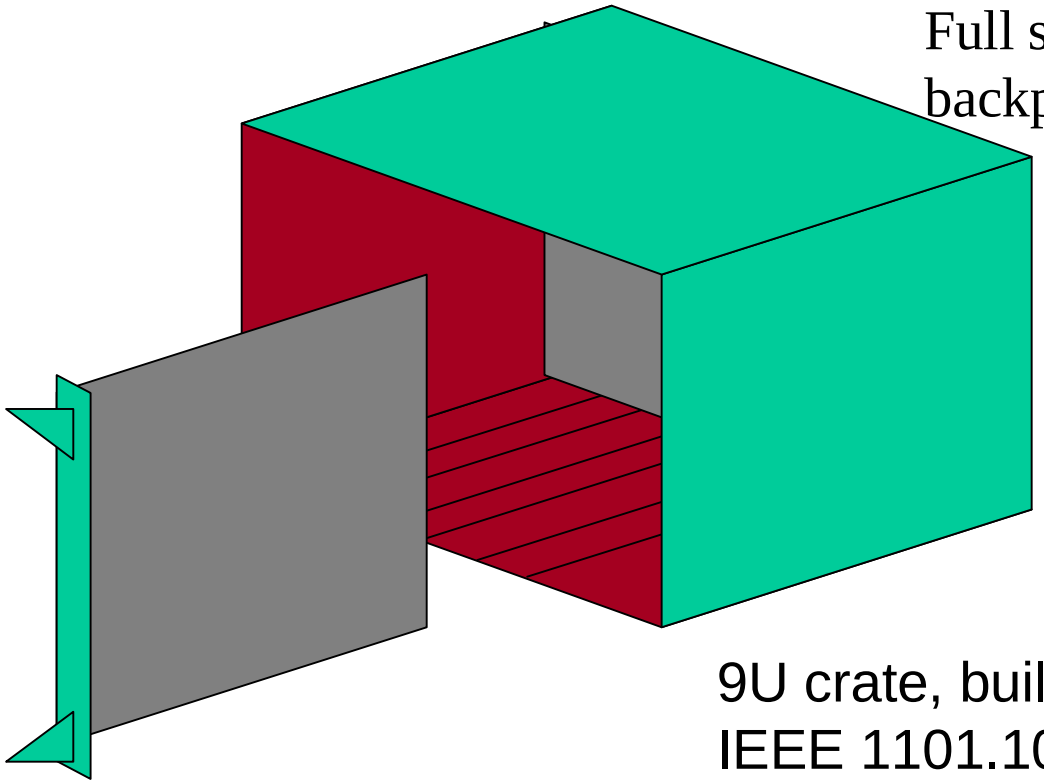
Merger Modules

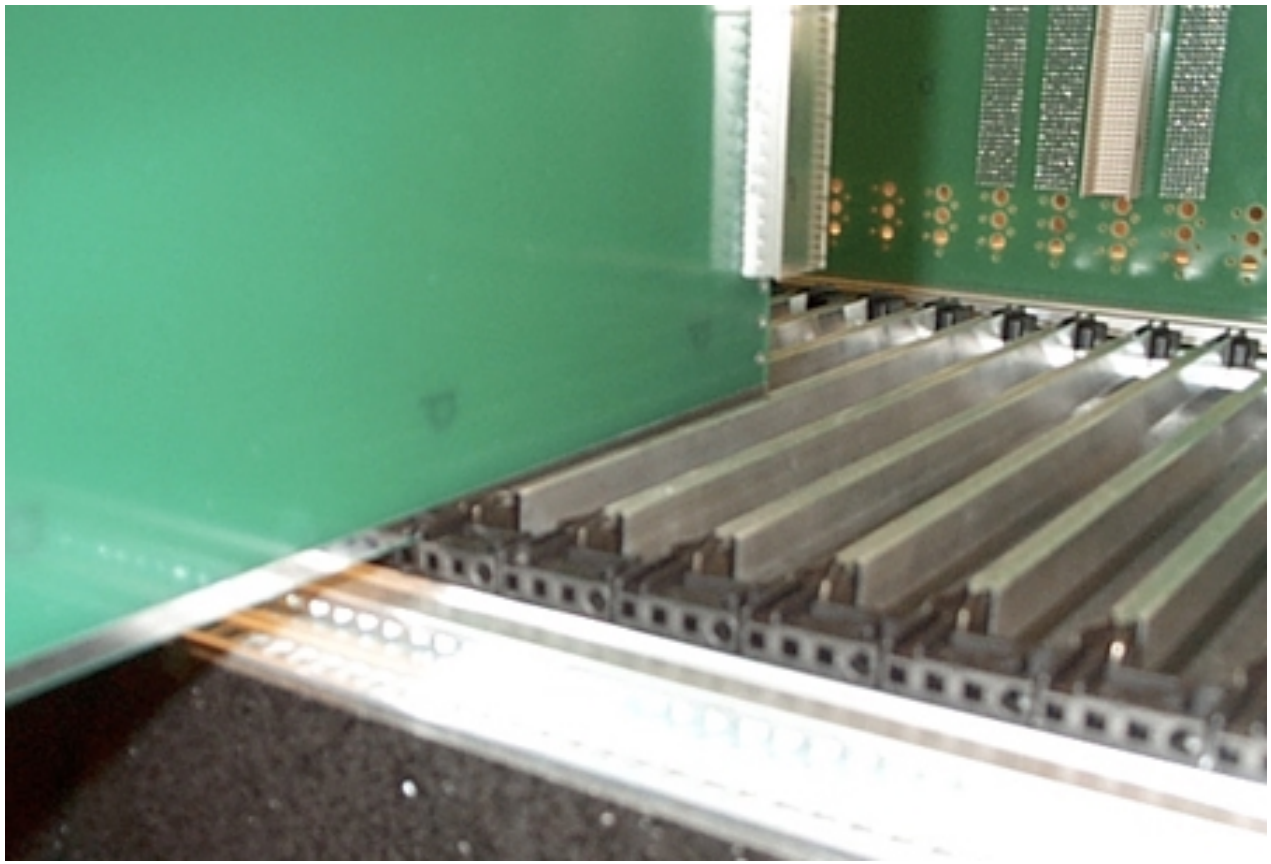
TTC connections

We are currently in contact with a backplane manufacturer

- Bustronic Corp., Fremont CA USA
  - www.bustronic.com
  - Specialize in VME, CPCI, and custom backplanes
  - Partnership with ELMA
  - Positive reaction, small orders no problem
  - Preliminary quote soon

We have built a crate mechanics demonstrator





The demonstrator can be considered a pessimistic test

- Backplane thickness
  - Demonstrator: 3.2 mm, no copper.
  - Final: 4.7mm, 8 ground planes
- All pins are the same height
- Pin alignment
  - Demonstrator: 0.8mm holes, hand placement
  - Final: 0.6mm holes, machine press-fit

First results from demonstrator

- Insertion/extraction tests with 2/3 shields worked!
  - Straightforward insertion/extraction of daughter card using both handles
  - Possible but difficult to extract using only one handle (asymmetric)
  - No discernable wear on handles after 30 cycles

Some observations

- Bracing hardware behind the backplane is necessary
- Guide pin appears to provide good alignment during insertion
- Don’t forget ESD features in module design!

Still to be done

- Insertion/extraction forces
  - Complete the installation of backplane and daughter card connectors
  - “Torture test” of hardware to failure
- PCB integrity
  - Investigate stiffening hardware designs for backplane and daughter boards

Schedule and milestones

- Mechanical demonstrator
  - Ongoing tests in parallel with design of the prototype processor backplane
- Prototype PB
  - Project specification draft available now
  - PDR November 20 at Mainz
  - Start layout soon after PDR is finished