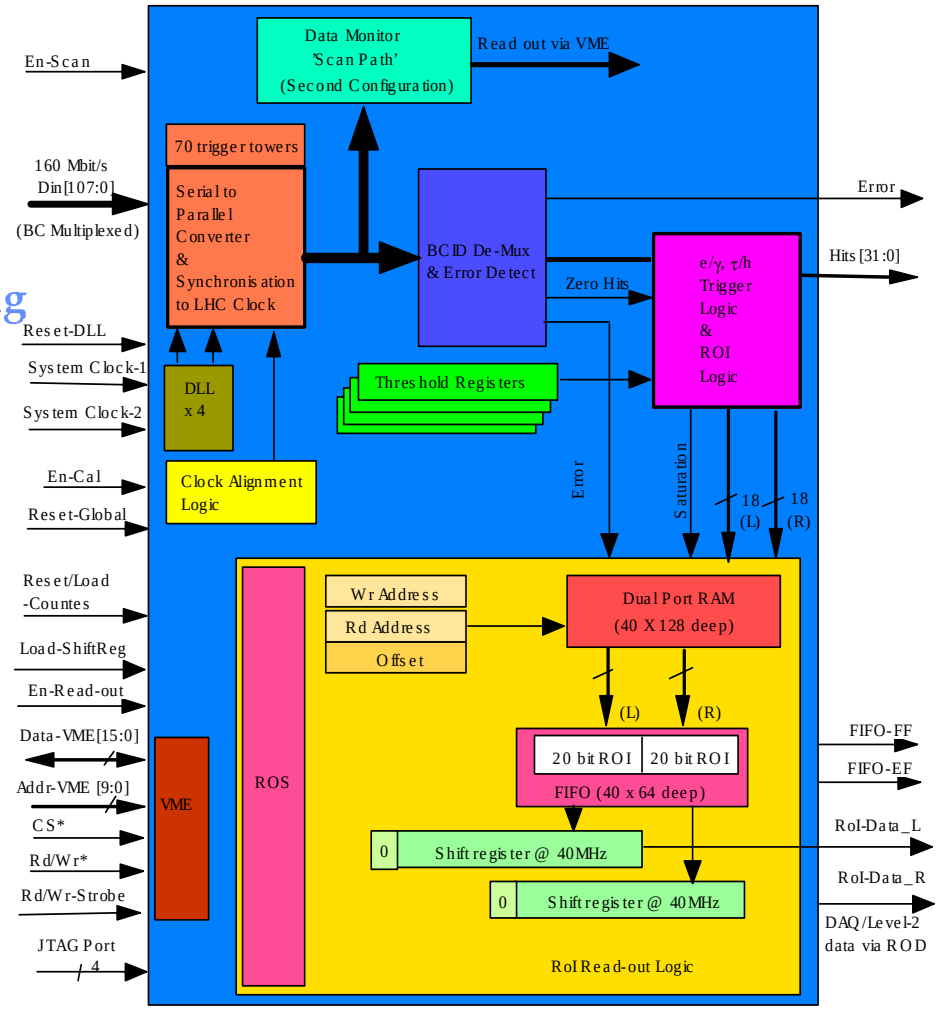
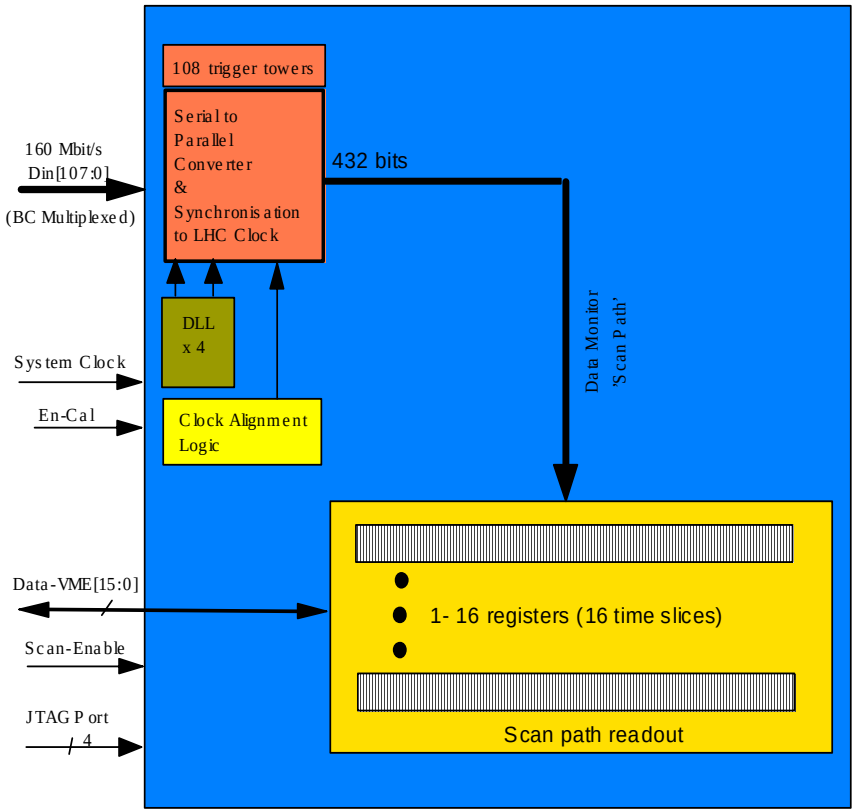
Cluster Processor Chip

- **Requirements**
  - Process 4 x 2 x 2 TT Window
  - Receive BC multiplexed data
    - **108 at 160 Mbit/s**
  - Capture and synchronise
  - BC-De mux and error checking
  - e/γ, τ/h Algorithm
    - **Cluster Hits**
    - **RoIs**
  - Readout of RoIs



Cluster Processor Chip

- **Requirements**
  - Set-up and diagnostic Logic (second configuration)



Cluster Processor Chip

- **CP Chip Status (2/11/00)**
  - **All logic blocks designed**
    - **Serial to Parallel conversion and Synchronisation**
    - **BCID De-multiplexing logic**
    - **Algorithm**
      - **Simulated with test vectors provided byAlan**
    - **Readout logic**
  - **In the process of integrating the logic blocks**
  - **Set-up and diagnostic logic implemented as a second configuration**

Cluster Processor Chip

- **Target devices - Xilinx XCV1000E or XCV1600E**

Configurable Logic Block (CLB) count for CP Chip

Logic Block	CLBs	Comments
Serial to Parallel	0478	Designed
BCID-De-multiplex	0378	Designed
RoI Read-out	0071	Designed
Algorithm	3904	Designed
Scan Path (spy)	(2900)	Re-configure FPGA
Total	4831	CLBs before integration

Available CLBs and I/O in Xilinx Virtex-E

	XCV600E	XCV1000E	**XCV1600E**	XCV2000E
CLBs	3456	6144	**7776**	9600
Utilisation		~ 79%	**~ 62%**	~ 60%
I/O	512	512	**512**	512
Utilisation		~ 40%	**~ 40%**	~ 40%

Cluster Processor Chip

- **Latency**
  - **Six ± 1, 40 MHz clock ticks (estimated from individual blocks)**
- **More Test vectors needed to complete the design**
  - **Test bench with Serialisers**
  - **Input data for the Serialisers**
    - **Work from Alan's test vectors for BC multiplexed data**