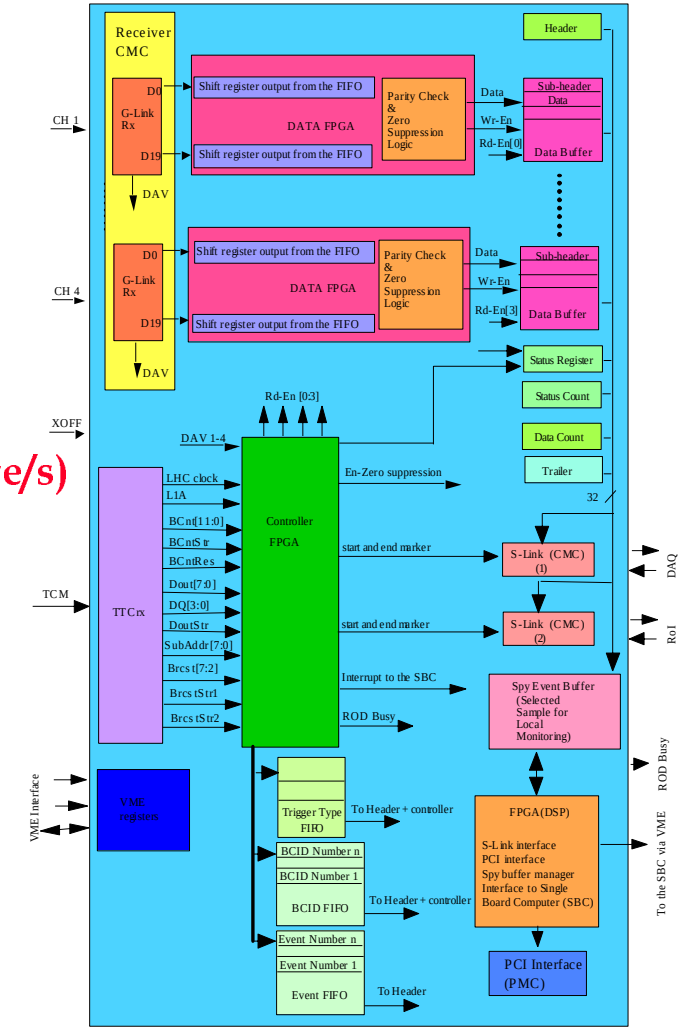
Prototype ROD

- Prototype ROD (6U VME)
  - Requirements
    - 4 channel (CPMs) prototype
    - Perform zero suppression
    - Perform parity check
    - Format data
    - Buffer formatted data
    - Readout via S-Link (160 Mbyte/s)
    - Spy on 'Events' transferred

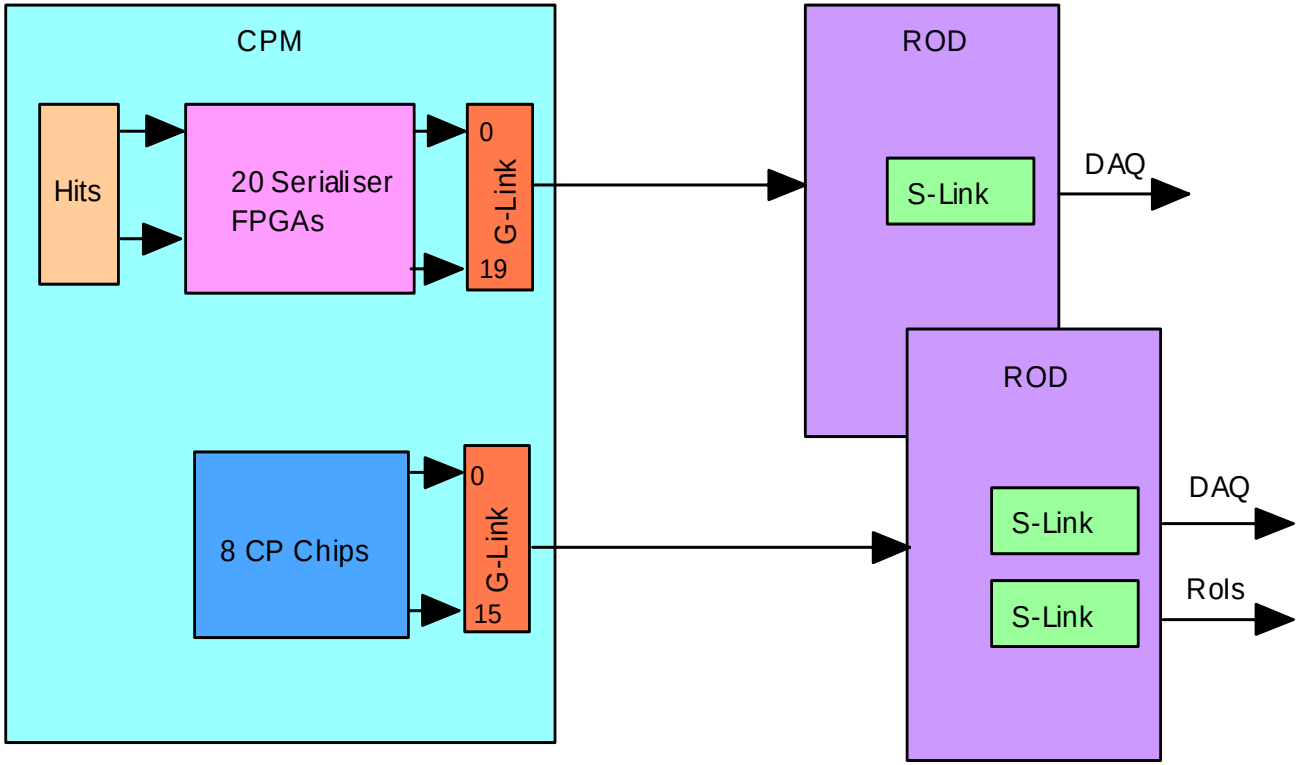


Prototype ROD (CP/Jet)

- **Prototype ROD - Implementation**
  - Receive data via G-Link CMC daughter card (4 channels)
  - All processing and data handling carried out by FPGAs
  - FPGAs developed to handle the Serialiser data (DAQ)
  - Same module with different FPGA firmware will handle RoIs
  - Off-the-shelf S-Link card to transfer data out
  - Spy on events for monitoring
    - Buffer four events
    - Data available for a PCI Mezzanine Card
  - TTCdec card to interface to TTC system

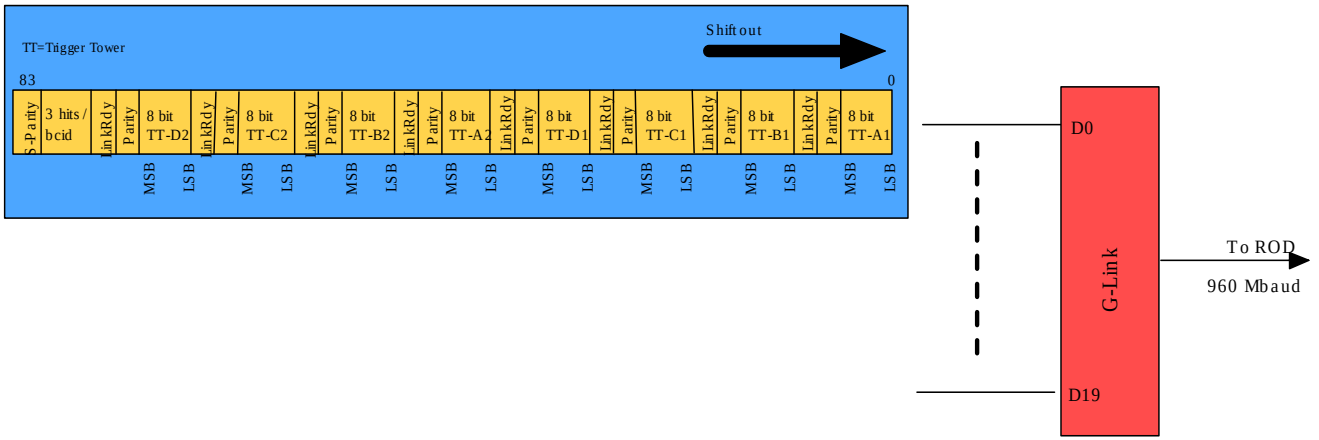
Prototype ROD (CP/Jet)

- Data from CPMs



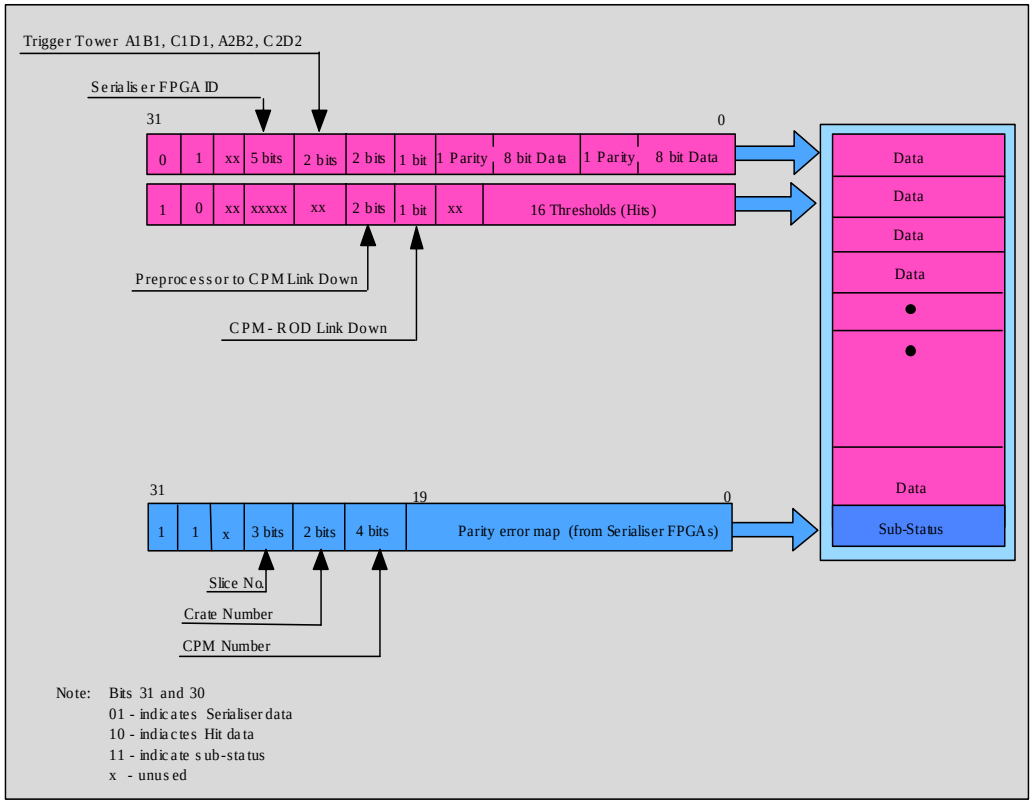
Prototype ROD (CP/Jet)

- Serialiser data (20 serialisers/CPM)



Prototype ROD (CP/Jet)

- Data received, formatted and buffered on the ROD



Prototype ROD (CP/Jet)

- Events transmitted to DAQ via S-Link
- Copy to spy buffer

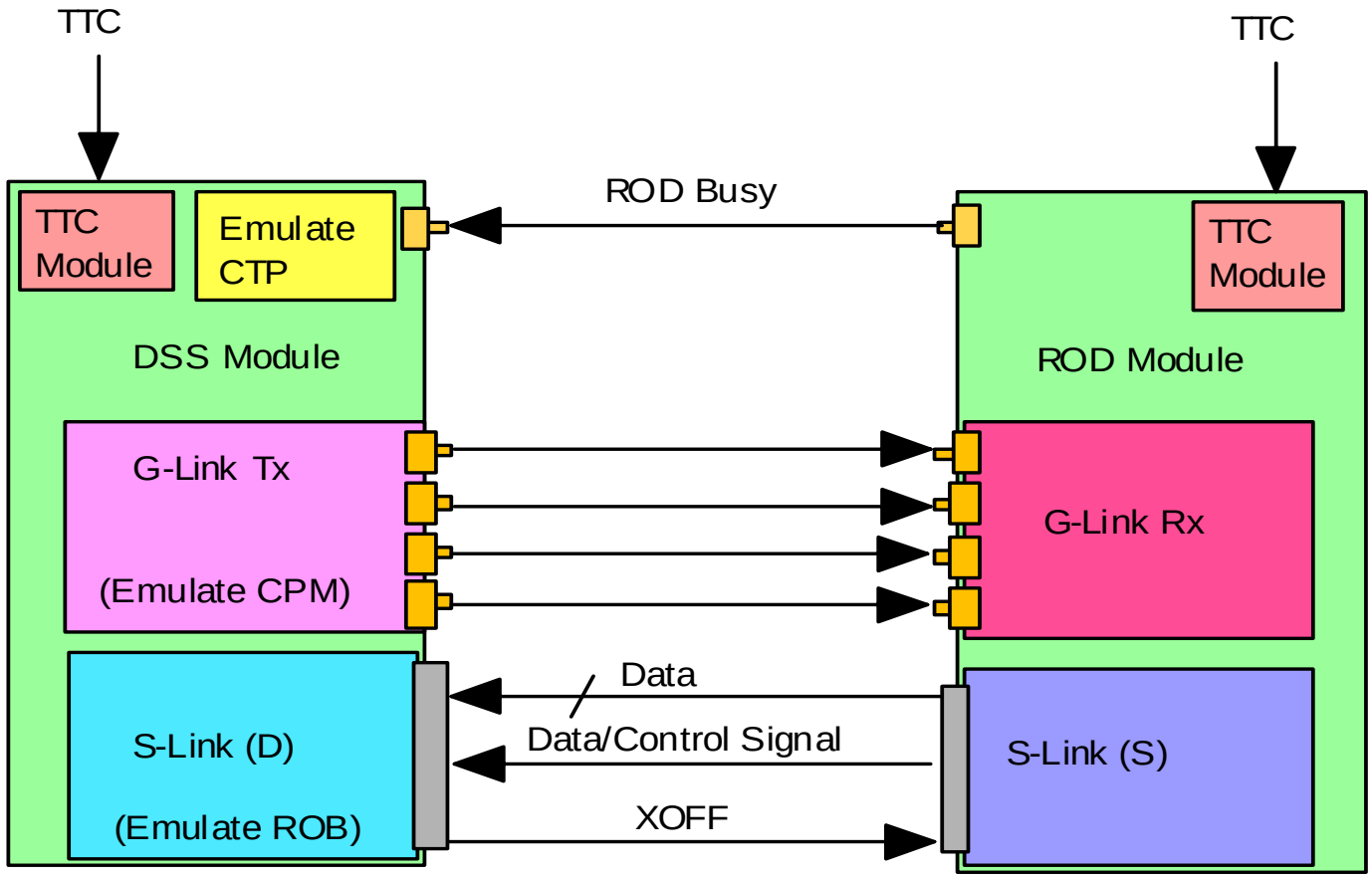
Content	Type
Begin of Fragment (B0F00000 Hex)	Control
Start of Header Marker (EEEEEEEE Hex)	Data
Header Size (0008 Hex - number of words in the header excluding control word)	Data
Format Version Number	Data
Source_ID - four byte field: [71][Crate ID][Module type][Module ID]	Data
ROD_L1ID (24 bit event)	Data
ROD_BCID (12 bit BCID)	Data
Leve1 Trigger Type	Data
Detector Specific Event Type (00000000)	Data
Data Words (from Data Buffers)	Data
Status Word-1	Data
Status Word-2	Data
Status Summary [31:16]/ Number of Status elements [15:0]	Data
Number of data elements	Data
Status block position	Data
End of Fragment (E0F00000 Hex)	Control

Prototype ROD (CP/Jet)

- Status (2/11/00)
  - Four modules manufactured
  - Two fully assembled and Boundary Scanned
  - One ROD under test now

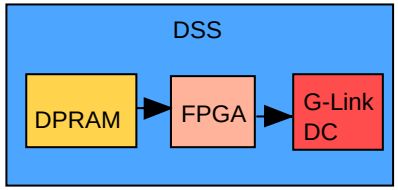
Prototype ROD (CP/Jet)

- Test Set-up



Prototype ROD (CP/Jet)

- Test status (2/11/00)
  - VME access is OK
  - Data transferred from a DSS ('CPM') to ROD
    - 'Serialiser data' in DSS firmware - fixed pattern
    - From DSS memory



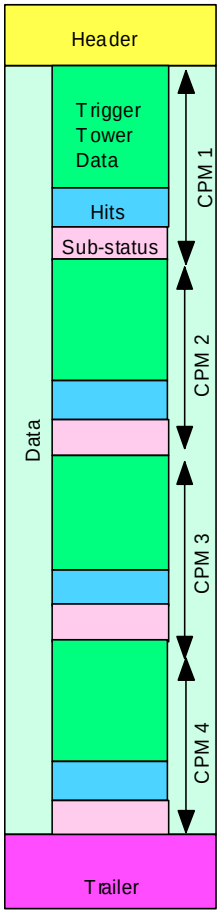
  - ROD receives data, format it and writes onto the FIFOs
  - Transfer 'events' via S-Link to a DSS ('ROB')
    - 'Events' received correctly on to the DSS memory
    - 'Events' captured on the spy buffers

Prototype ROD (CP/Jet)

- Results -Spy buffer, DSS memory

B0F00000			
EEEEEEEE			
00000008			
00000001			
00000001			
00000000			
00000000			
00000000			
00000000			
40822210	40A02712	40C02B14	40E22E16
41022210	41202712	41402B14	41622E16
41822210	41A02712	41C02B14	41E22E16
42022210	42202712	42402B14	42622E16
42822210	42A02712	42C02B14	42E22E16
43022210	43202712	43402B14	43622E16
43822210	43A02712	43C02B14	43E22E16
44022210	44202712	44402B14	44662E16
44822210	44A02712	44C02B14	44E22E16
45022210	45202712	45402B14	45622E16
45822210	45A02712	45C02B14	45E22E16
46022210	46202712	46402B14	46622E16
46822210	46A02712	46C02B14	46E22E16
47022210	47202712	47402B14	47622E16
47822210	47A02712	47C02B14	47E22E16
48022210	48202712	48402B14	48622E16
48822210	48A02712	48C02B14	48E22E16
49022210	49202712	49402B14	49622E16
49822210	49A02712	49C02B14	49E22E16
40022210	40202712	40402B14	40622E16
			8000FFFF
			8000FFFF
			8000FFFF
			C4000000
			X four blocks
			0
			0
			2
			150
			1
			E0F00000

‘Event’



Prototype ROD (CP/Jet)

- Next
  - Test with the TTC system
  - More tests!
    - Zero suppression
    - RoIs
    - Busy
    - Monitoring (PCI, VME single board computer), etc,
  - Get the second module up and running
  - Assemble other two modules

Prototype ROD (CP/Jet)