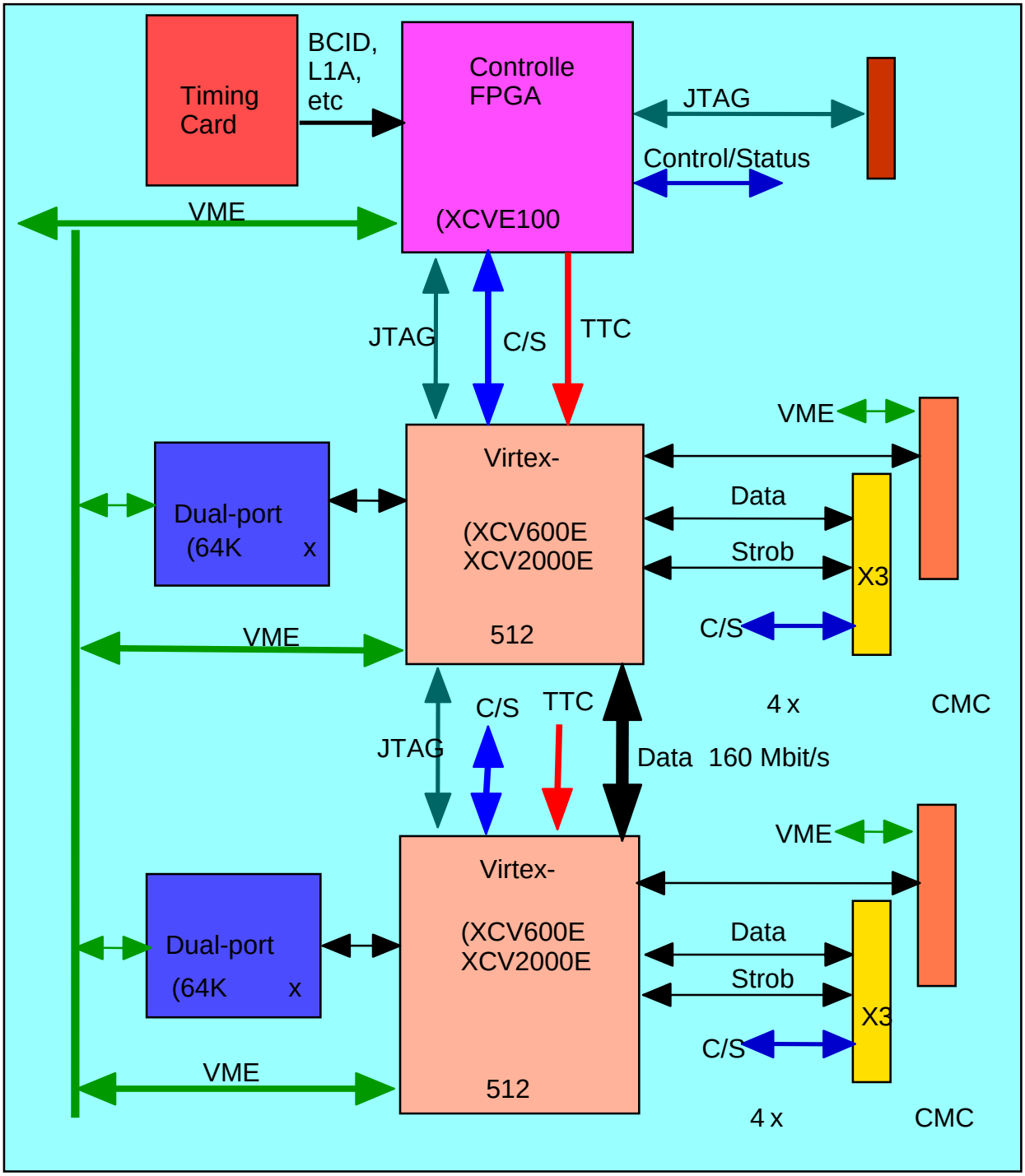
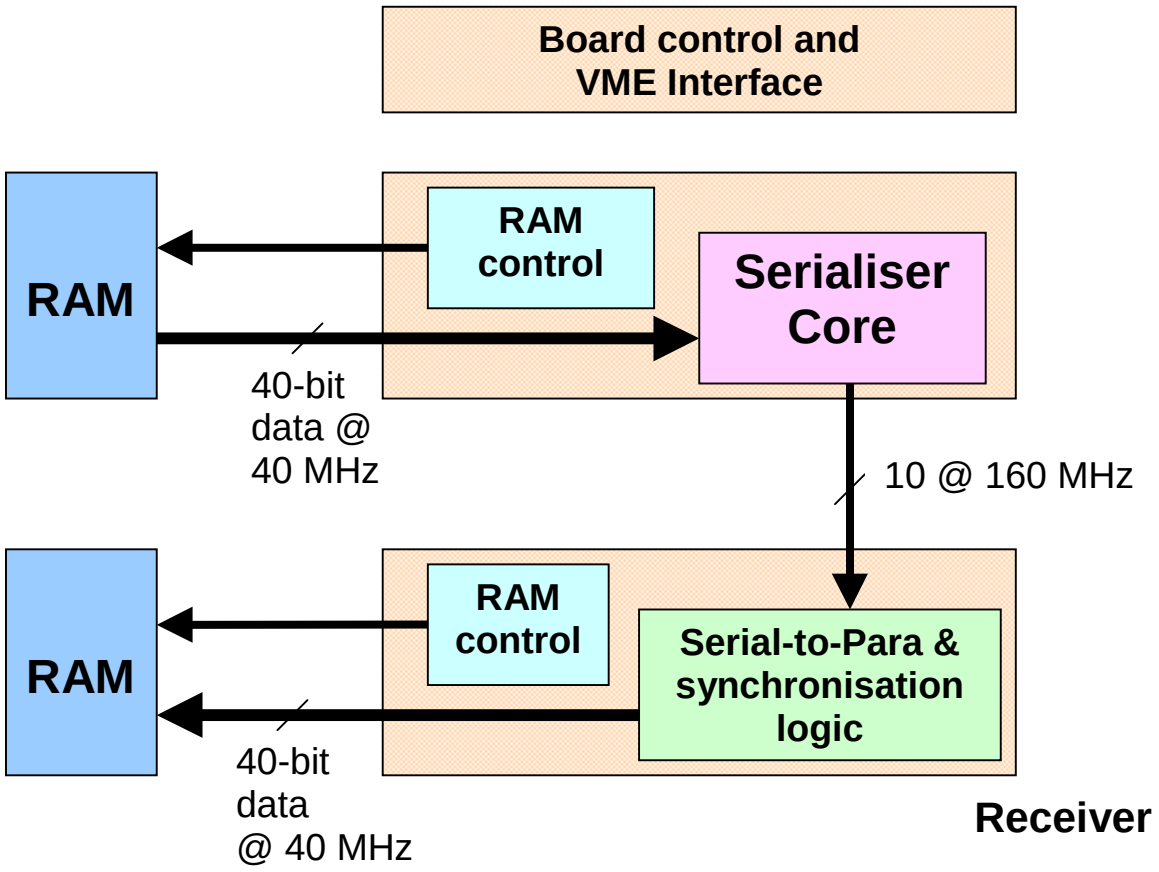
Status Report:
Serialiser; GTM for tests

Ian Brawn, 1-12-00.



Testing the Serialiser



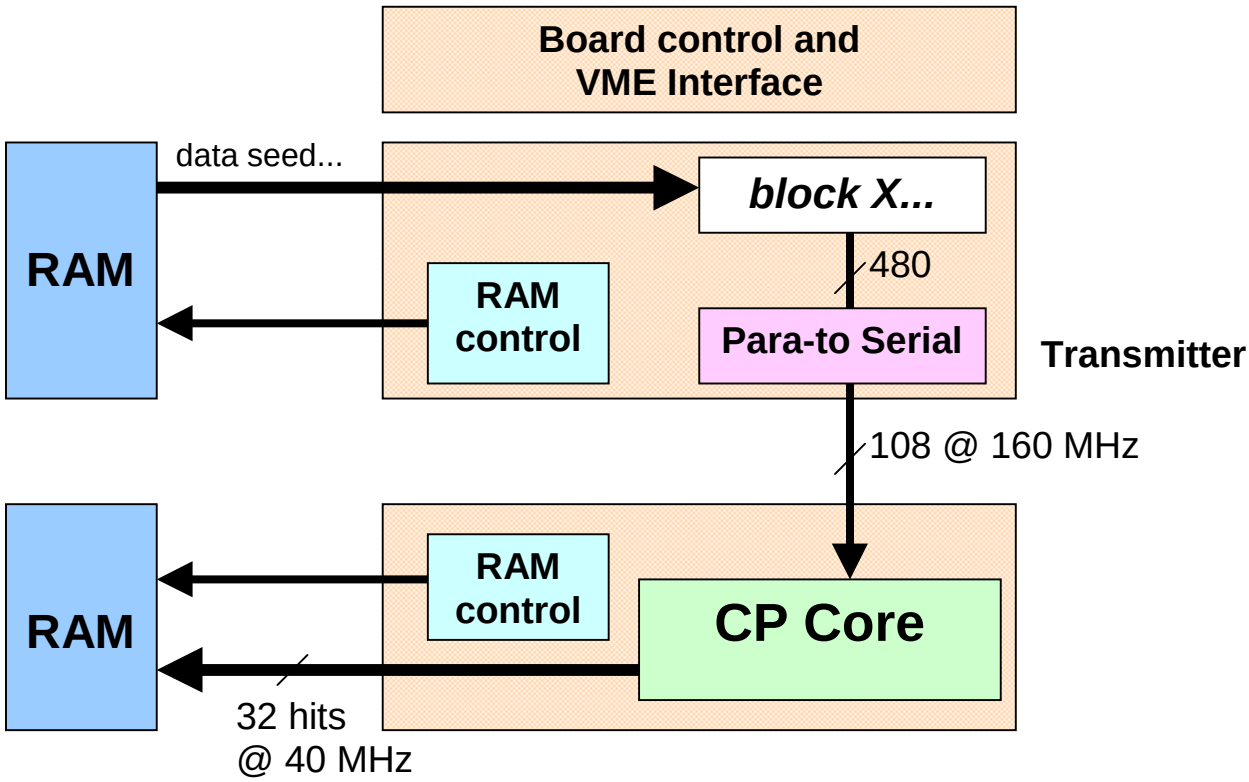
3 FPGAs to design:

Serialiser test configuration: existing Serialiser core with added logic to control RAM.

Receiver: Serial-to-Para and sync. logic built from components of CP front end.

Board control and VME decoding: modify existing logic designed by Azmat.

Testing the CP chip



3 FPGAs to design:

Board control and VME decoding: modify existing logic designed by Azmat.

CP test configuration: existing CP core with added logic to control RAM.

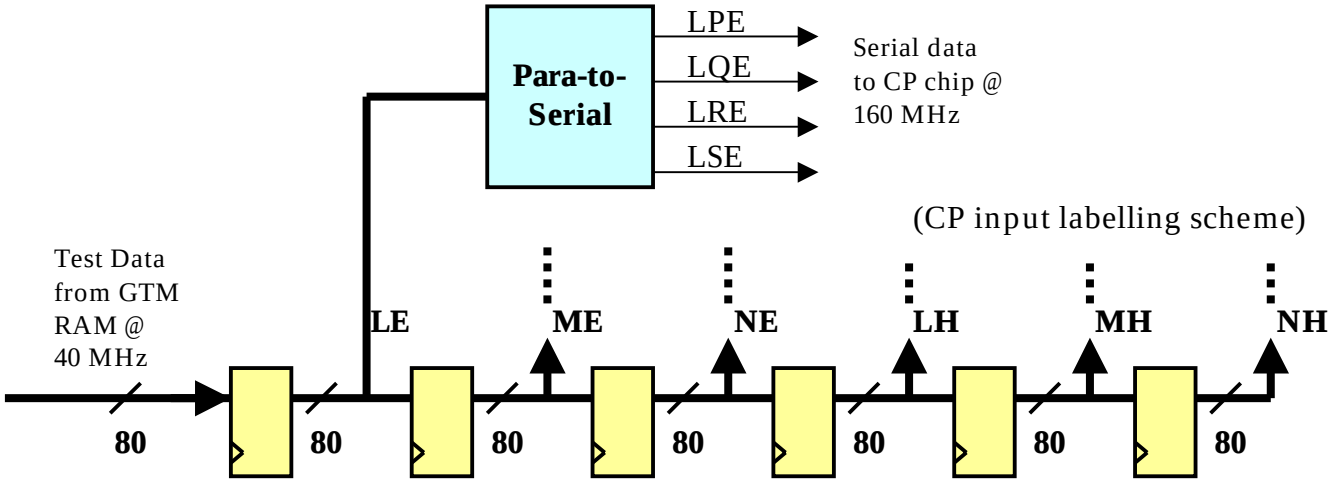
Transmitter: Serial-to-Para and sync. logic built from components of CP front end.

CP Transmitter

Provides CP chip with test data:

- 108 serial lines @ 160 MHz
- = 48 BC-muxed pairs
- ⇐ 480 parallel bits @ 40 MHz
  (GTM RAM width = 128 bits)

Use S/R to populate all serial lines:



- Allows sensible parity & BC flags to be set.
- Allows generation of history for BCMUX.

Status

GTM: ?

Serialiser Test Bench

- Serialiser complete
- Receiver complete
- VME interface to be done

CP testbench

- CP chip to be done
- VME interface to be done
- CP chip - pin out and timing to be done

All of test bench firmware should be ready when required.