Status of LVDS link tests at Birmingham

Tests with LVDS sink card -2.

2 daughter cards received;
Sn #5 has fault on 1 channel - data path.
Sn #6 used in tests ⇒

Using 2 x 12.5m of Datwyler cable lengths with 33 Ω + 100 nH precompensation.

Without TTC:

Test run for 22hrs overnight, 3 x 10^{13} bits each:

6/8 links were error free
1 link had 1 error
1 link had 2 errors error rate < 10^{-13}

With TTC:

Test run for over 2 hours, 3 x 10^{12} bits each:

7/8 links were error free
1 link had 3 errors error rate < 10^{-12}

(more statistics needed)

Status of LVDS link tests at Birmingham

New LVDS source card -2

Design Specification written:

http://www.ep.ph.bham.ac.uk/user/staley/lvds_spec2_1.ps

To include:

- Supply filter
- High Stability PLLs on incoming clocks
- LVDS Fanout chips - now 2 choices:

Texas Instruments SN65LVDS104

http://www.ti.com/sc/docs/products/analog/sn65lvds104.html

National Semiconductor DS90CP22M

http://www.national.com/pf/DS/DS90CP22.html

LVDS Fanout Demo PCB

Layout by Simon Pyatt , Birmingham.
PCB due this week from PCB-POOL.

Contains single LVDS link, clocked by Hi-Q PLL and using Texas LVDS fanout device.

Results from this will feed into DSS / LVDS Source CMC design.

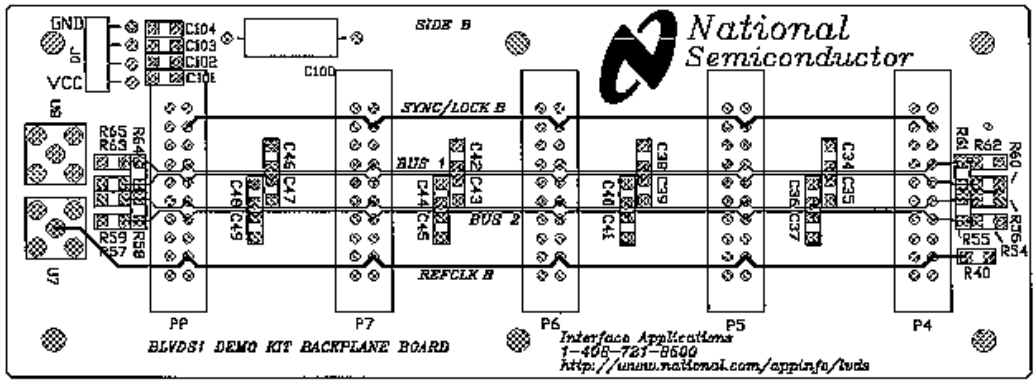
Finally, on digging around National Semi's web site , a note relating to their LVDS Demo PCBs:

http://www.national.com/appinfo/lvds/files/BLVDS01_02_REV.pdf

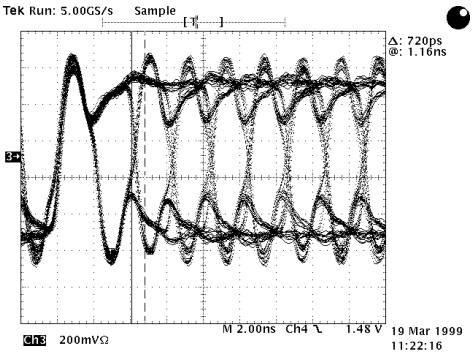
Using the BLVDS Demo Kit

The BLVDS Demo Kit was designed to allow the user to observe the operation of the DS92LV1021 serializer and either the DS92LV1210 (Order # : BLVDS01) or the DS92LV1212 (Order # : BLVDS02) deserializer. Several configurations are possible. With the purchase of additional kits multidrop applications can be modeled.
The kit consists of a backplane card with 4 differential busses, 2 DUT cards; one configured as a serializer and one configured as a deserializer, and 4 adapter cards which can be used to adapt the pin header I/O of the DUT cards to SMB or SMA connectors.

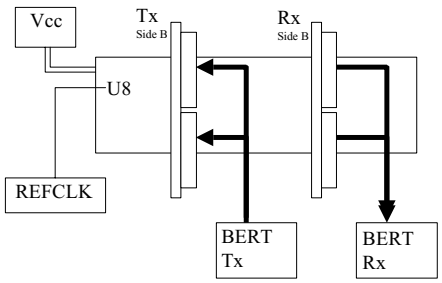
The Backplane card



Each side of the backplane card has 2 differential busses, a REFCLK bus to distribute the REFCLK signal to deserializer cards, and a SYNC/LOCK bus that connects the LOCK* output from deserializers to the SYNC1 input of the serializer.
Each differential bus is designed for a target unloaded impedance of 130 ohms. Since addition of DUT cards and load capacitors will lower this impedance the busses are terminated in 100 ohms at each end. Each differential bus has 5 ‘slots’ which use 20 pin dip headers to insert DUT cards. Between each of the slots there are provisions for adding capacitors to simulate extra loading on the bus. As the bus configuration is changed by adding additional DUT cards or by adding load caps on the bus the termination resistors should be changed to match the loaded impedance of the bus.



Typical Configuration

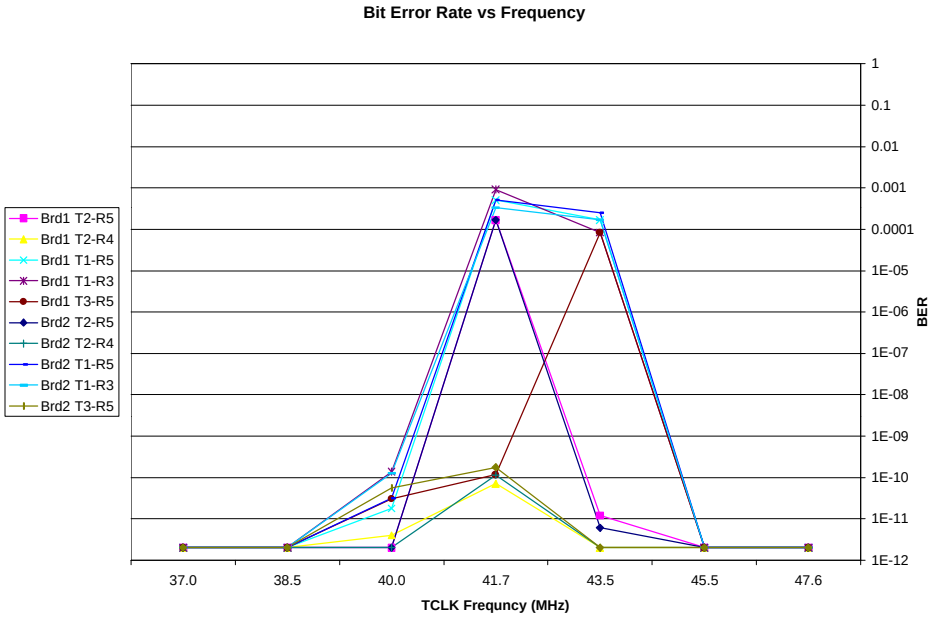


Updates for Using the BLVDS Demo Kit

24 May, 1999

1.0 Bit Error Rate vs. TCLK frequency

When operating the demo kit as a backplane certain problem frequencies have been observed. Basically the Bit Error Rate is high in the range from 39 MHz to 44 MHz base clock frequency for the DS92LV1210 and 38MHz to 50MHz clock frequency for the DS92LV1212. The kit will operate normally above or below this frequency range. Chart 1 illustrates the BERT results for 2 demo kit backplanes with the Tx and Rx cards placed in various slots.



2.0 Excessive Supply Current Drawn by the Demo Kit

When operating the kit draws excessive supply current – more than would be expected for just a Tx, Rx and a hex inverter. The excess current is drawn by 2 pull-up resistors connected to the hex inverter outputs. Changing resistors R36 and R41 from 75 ohms to 1Kohm or greater will significantly reduce the supply current drawn by the demo kit.