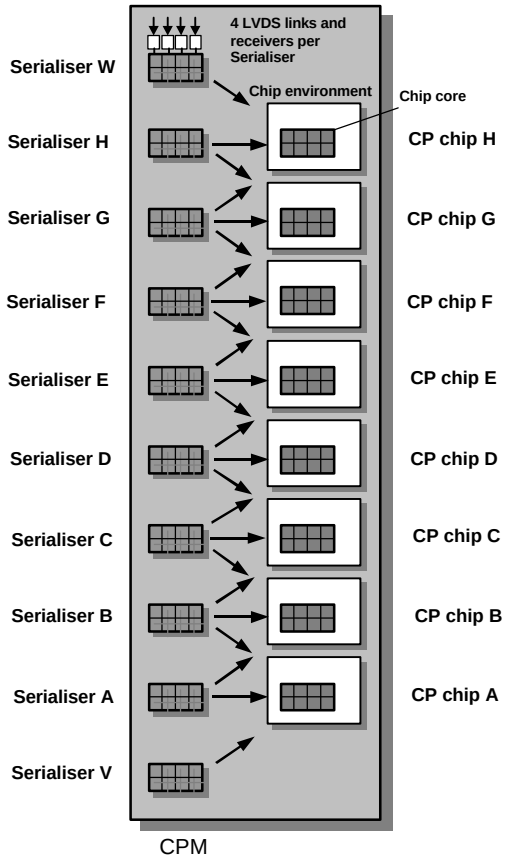
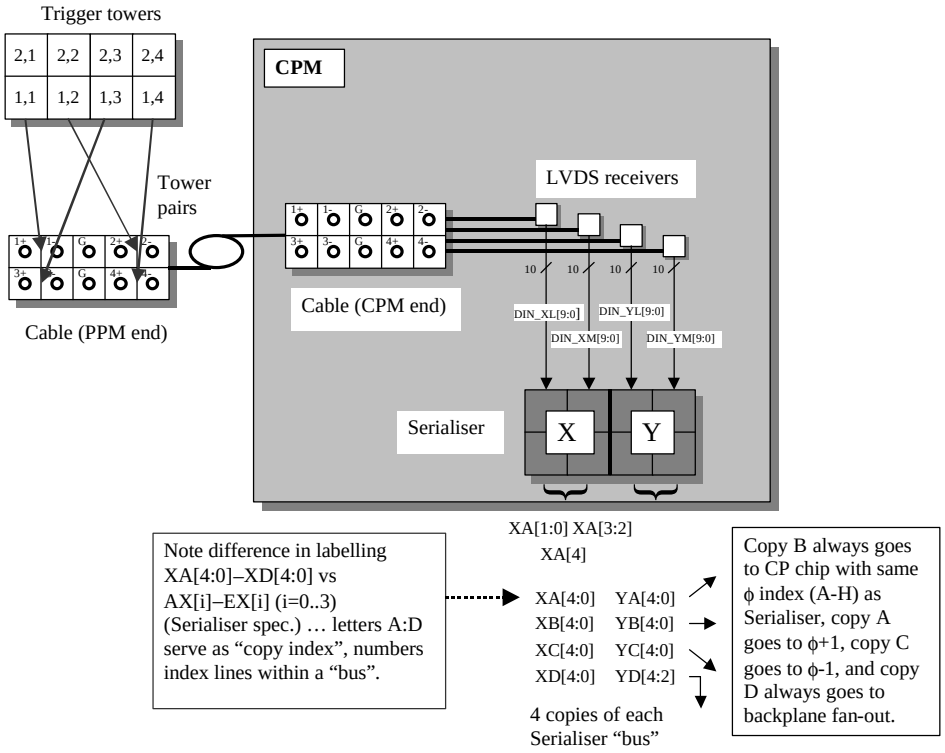
CPM Organisation and labelling

- Labels needed for CPM signals and CP chip pins
- Mappings between devices, no harm in clarification
- Some (obvious) CP chip pin assignments



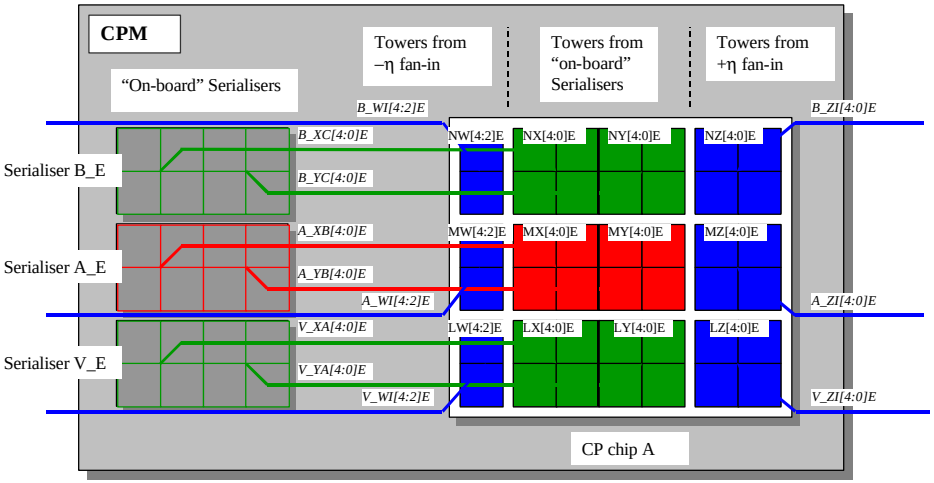
Serialiser I/O

- Assign tower pairs to cables
- 2 Serialiser halves, X & Y
- Assign tower pairs to inputs
- Tower pairs output on output “bus” [4:0] – line 4 flag+parity
- Each bus has 4 copies, 3 for on-board, 1 for BP fan-out
- Change Serialiser labelling for clarity (CAD compatibility?)



CP chip signals and pins

- Inputs from 6 on-board Serialisers (3 em+ 3 had), plus -/+η fan-in
- Label pins by source Serialiser as L(ower), M(iddle), N(orthern)
- Keep X and Y (left and right)
- Fan-in as W (-η) and Z (+η)
- Bus lines labelled [4:0] (–η fan-in [4:2] only)
- Append E or H (em/had)
- Label signals by source Serialiser ϕ index + X/Y + copy index A-C
- Fan-in given copy index I



NB. Signal labels (italics) and pin labels (roman) shown for electromagnetic data only (appended "E"). All labels re-used for hadronic data with appended "H".

CP chip pin labels

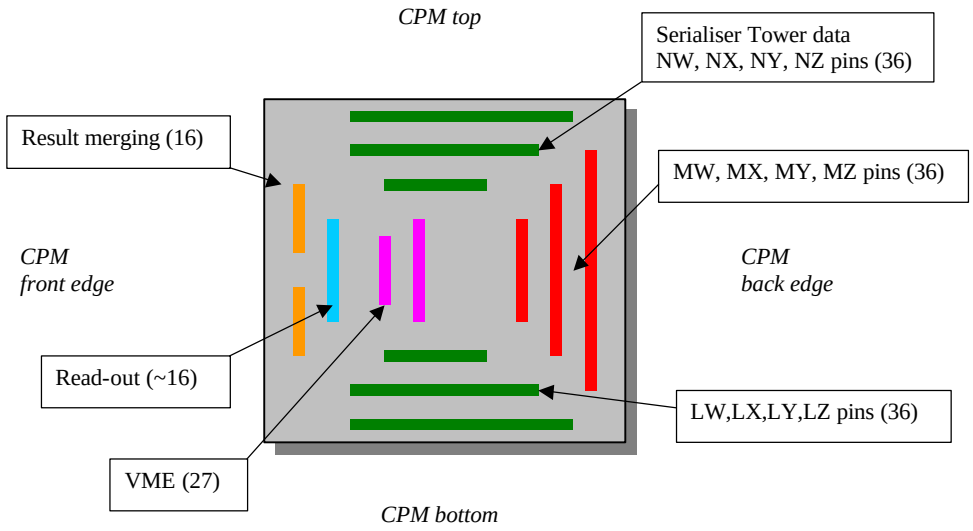
NW[4:2]E NX[4:0]E NY[4:0]E NZ[4:0]E

MW[4:2]E MX[4:0]E MY[4:0]E MZ[4:0]E

LW[4:2]E LX[4:0]E LY[4:0]E LZ[4:0]E

CP chip pin-out

- Given a choice … inputs one side and outputs opposite
- 108 inputs vs 32 outputs (real-time only)
- Put Serialiser-sourced inputs closest to source Serialiser!!
- Keep read-out signals together (sourced from ROC)



Suggested CP chip pin-out