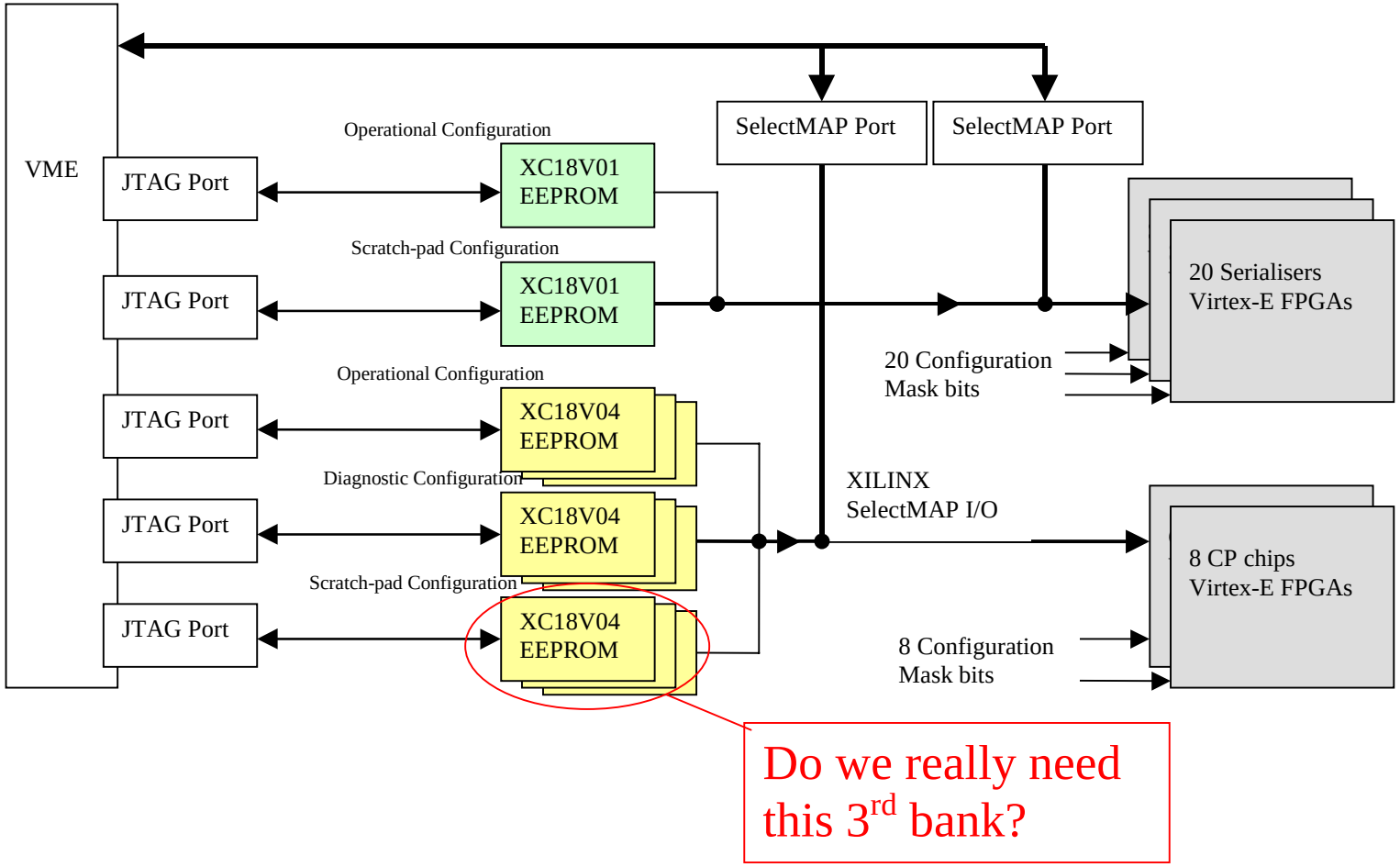
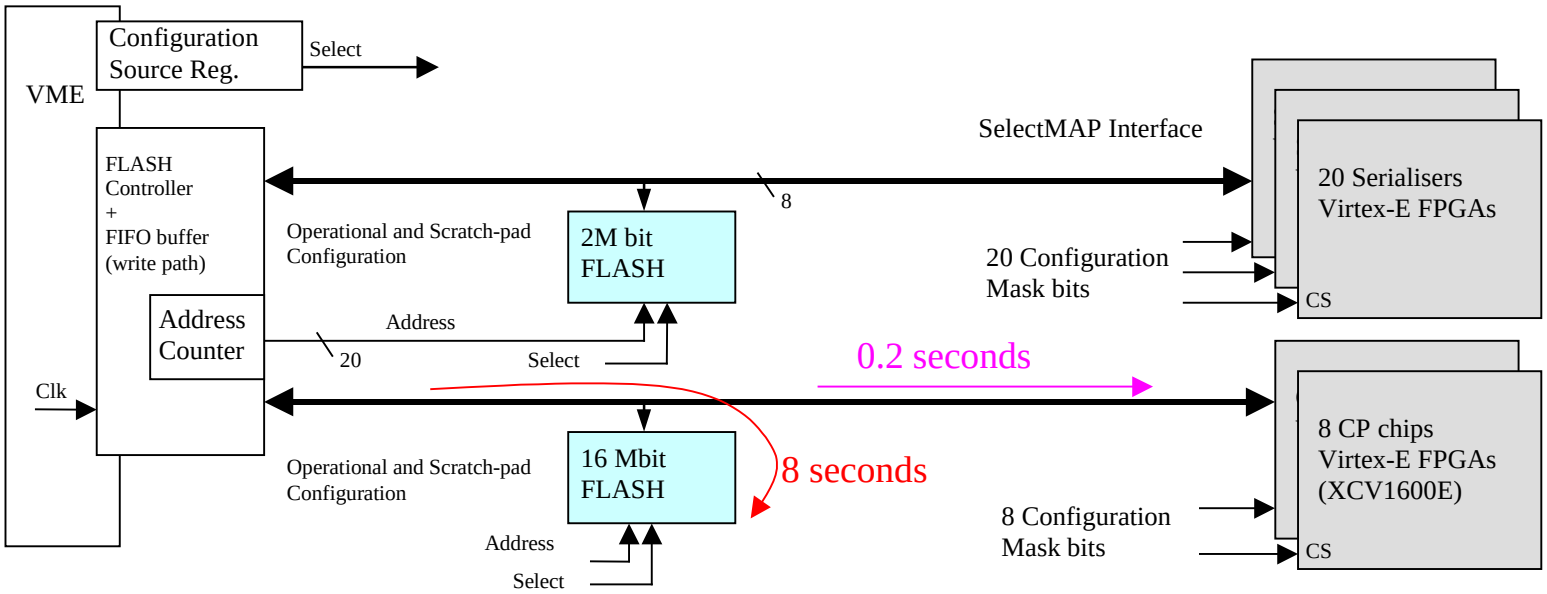
CPM - VIRTEX FPGA configuration - FLASH EPROM or XILINX JTAG?.

Present scheme using XILINX JTAG memory. (PDR).



Proposed scheme using FLASH Memory

2 'Local' Configurations for XCV1600E devices.



.

FLASH Memory vs Xilinx JTAG memory

	FLASH	Xilinx
Access	Byte serial via FIFO	Serial , through JTAG port
Cost	4 Mbit AM29F040B: $7 8 Mbit AM29F080B: $15	1 Mbit XC18V01: $15 4 Mbit XC18V04: $30

- I (We?) don't know how to program memories using a JTAG interface from VME.
- Using FLASH memory to hold Virtex configuration data is perfectly acceptable. XILINX Application note: XAPP137.
- Cost. Each CP chip configuration uses 10Mbits $\rightarrow$ 9 devices
  CP + Serialiser $\rightarrow$ 200 UK Pounds (Xilinx).
- Fewer devices

FLASH Programming times.

- A single location may take up to 300us to program, but typically 7us.
- The Am29F016D Flash memory will typically take 32 seconds for a complete **erase** and then 10 seconds to **program** with new CP FPGA configuration data

  $\rightarrow$ A FIFO buffer (256byte?) in the data path will allow the CPU to attend other duties while data is being written to the FLASH memory.

Thus the time take to change FPGA configuration data for a module, and for a full crate of modules ,will be typically **43 seconds**.

XILINX VIRTEX FPGA configuration from FLASH EPROM

Do we really need Serialisers to hold different configurations