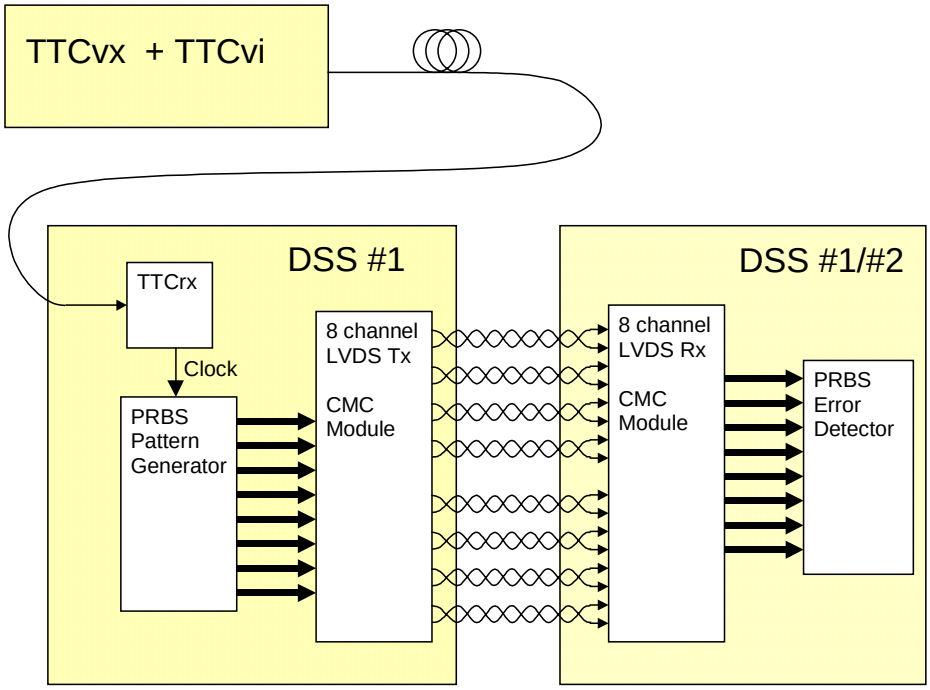
LVDS Link Tests at Birmingham

LVDS Link evaluation used the Data Source and Sink (DSS) VME modules clocked from a TTC test system:



Results using the original LVDS deserialiser DS92LV1210 operating at 40MHz (maximum frequency) showed a low tolerance to power supply noise and clock jitter. $\rightarrow$

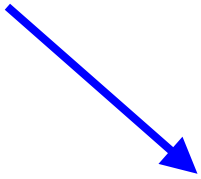
Error rates of $<10^{-12}$

These parts could only be used provided:

- Transmitters were clocked from a high stability source.
- Receiver supplies were heavily filtered.
- Cable HF loss was over-compensated.

But then …

… A faster LVDS chip-set was released, operating at 40 - 66MHz word rates.



Parameter	Original device DS92LV1210	New device DS92LV1224	Just released DS92LV1212A
Frequency range	16 - 40MHz	40 - 66MHz	16 - 40MHz
Data Timing margin (min)	100ps	450ps	450ps
Receiver Threshold (max)	100mV	50mV	50mV
Power consumption (typ)	145mW	191mW	191mW
Latency	1.75 T	1.75 T	1.75 T

- The later devices have a much improved timing margin on incoming data when compared with the original part.

Test results

LVDS link tests were repeated using the faster 40 - 66MHz Deserialiser part (DS92LV1224)

Several overnight tests on were run on various cable assemblies:

15m of High-density AMP cable
20m of Datwyler cable.

No errors were detected

3×10^{13} bits were sent over each link.

- These faster LVDS deserialisers do NOT need a high stability 40MHz clock source feeding the transmitter.

- Receivers tolerant of supply noise.

- The cable equalisation is relaxed, with particular component values now covering a much larger range of cable lengths.

Pic ’n’ Mix works, but we should keep to one chip set!

- The complimentary 40 - 66 MHz serialiser is not yet available in die form. $\rightarrow$ PPr MCM.

- An improved 16 - 40MHz deserialiser has just been released. Waiting for delivery quotes.

- Repeat Link Tests with system ’stressed’