CP FPGA 'Gate' Count

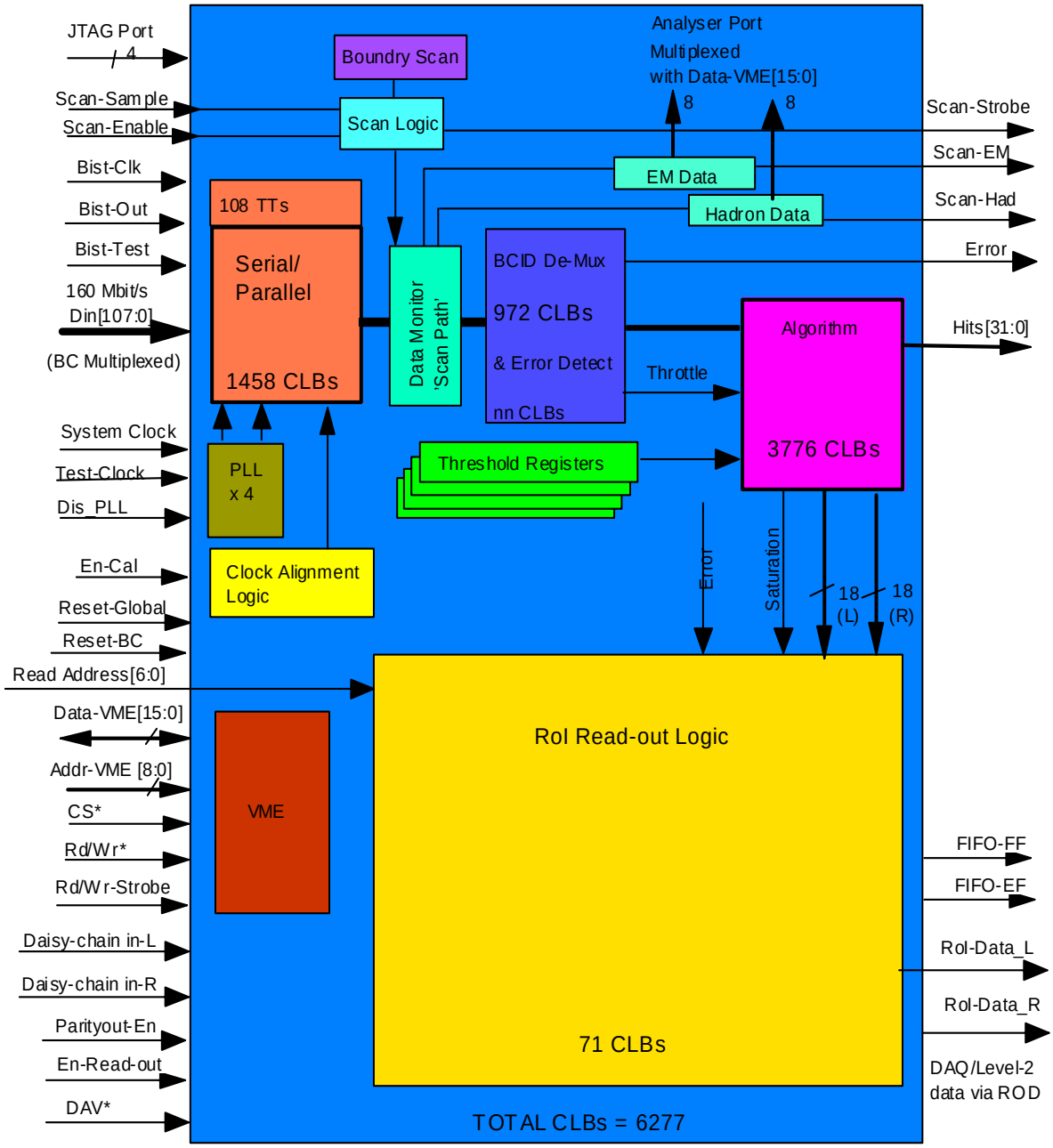

Figure 1. CLB Count

CLB count for CP FPGA

Logic Block	**CLBs**	**Comments**
Serial to Parallel	1458	Designed
Scan Path (spy)	0	Re-configure FPGA
BCID-De-mux	0972	Designed[1]
RoI Read-out	0071	Designed
Algorithm	3776	Estimate (see below)[2]
Total	6277	XCV2000E?

Note 1: Require error-checking logic

Note 2: CLB estimate for Algorithm block (optimisation not considered)

12-bit adders	= 576 x 3 CLBs	= 1728
8-bit comparators	= 1024 x 2 CLBs	= 2048
Total		**=3776**

Available CLBs in Xilinx Virtex-E

	XCV600E	XCV1000E	XCV1600E	XCV2000E	XCV2600E	XCV3200E
CLBs	3456	6144	7776	9600	12,696	16,224
Cost	£680	£1500				

Scan Path

To monitor the incoming data after serial to parallel conversion, The FPGA could be re-configured as shown in figure 2.

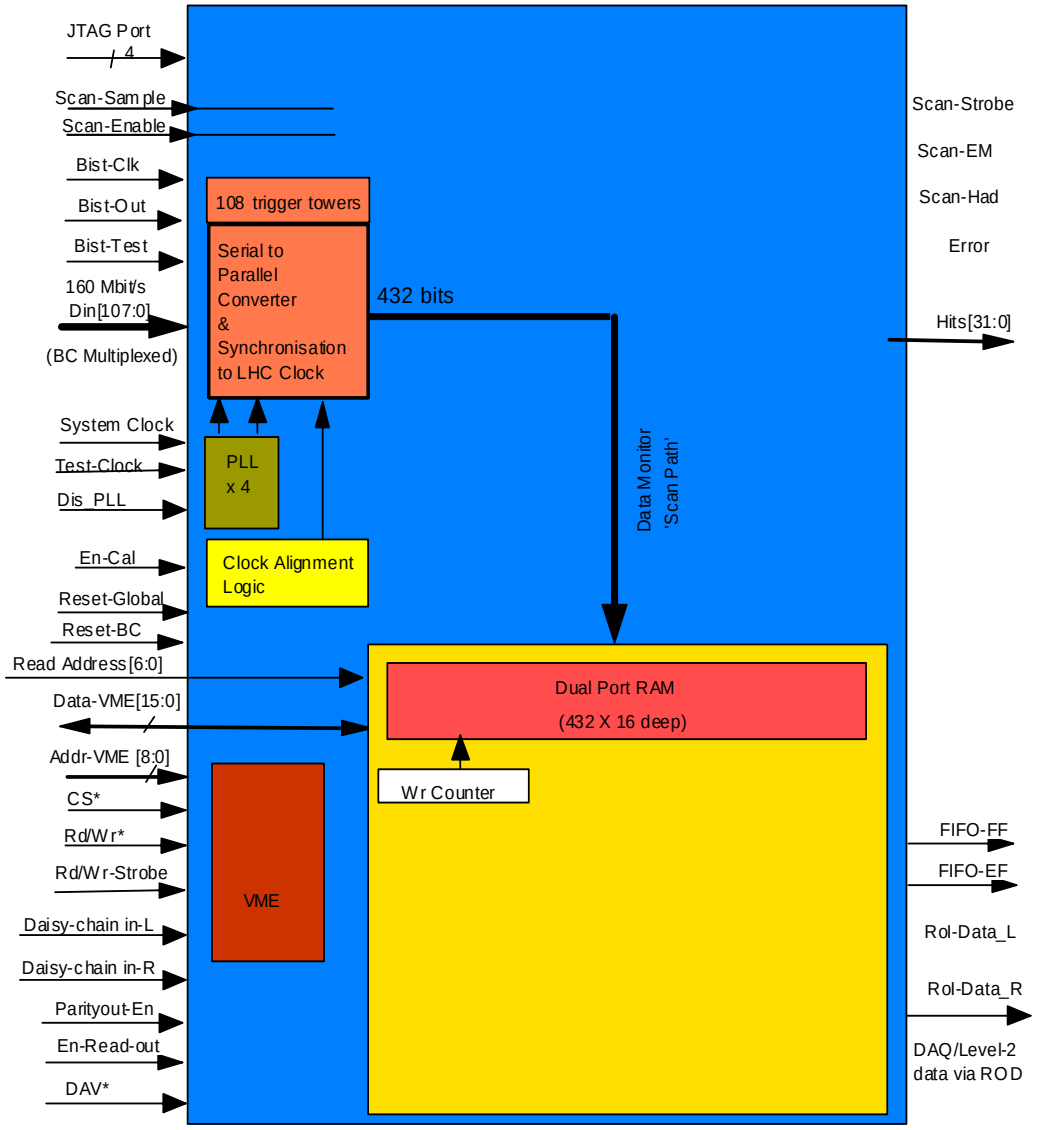

Figure 2. Re-configuration for input data monitoring

- 432 bits are captured on to a dual-port RAM
- n deep dual-port RAM
- Read-out via the VME?