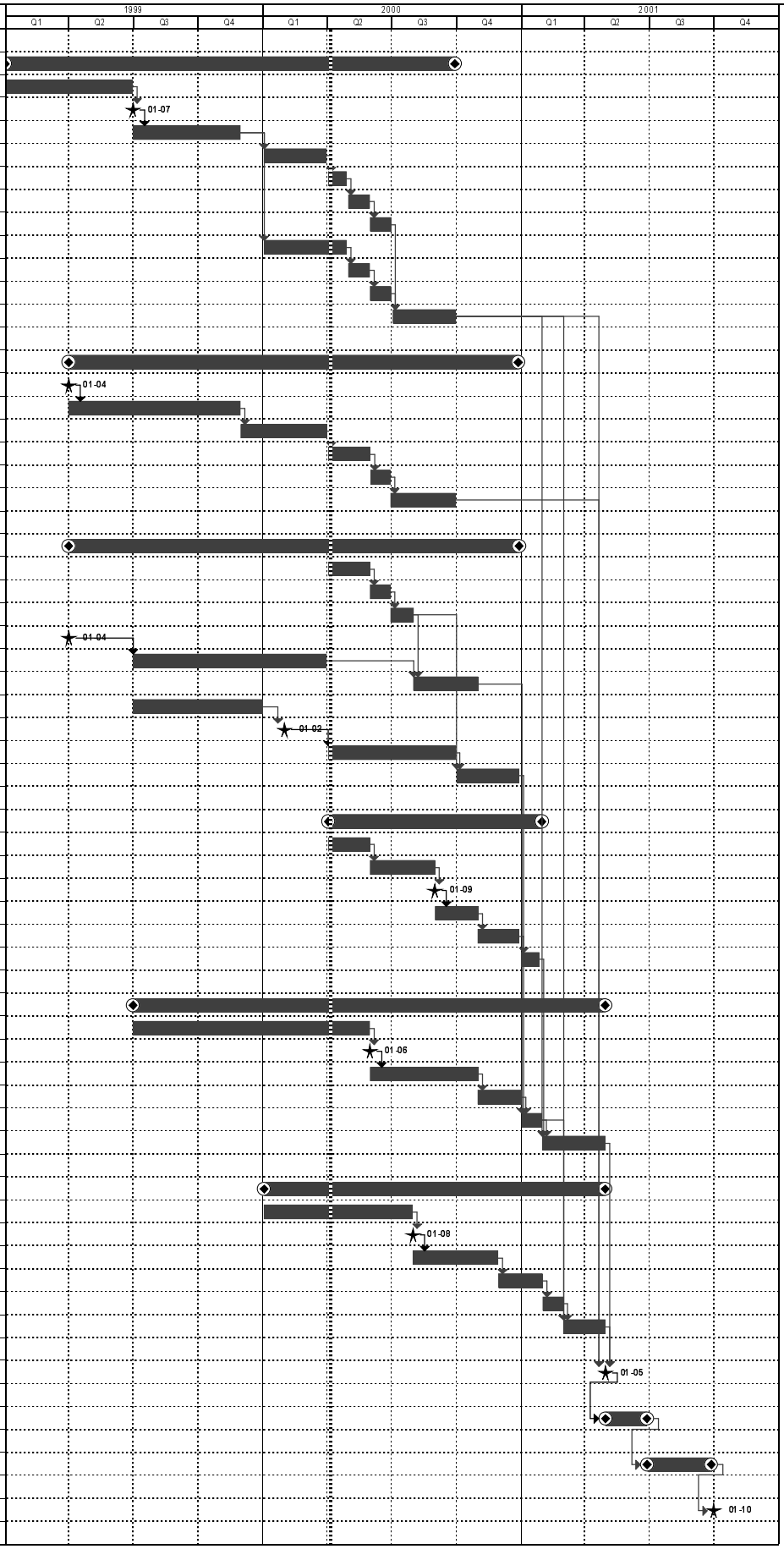
ID	Task Name
1	
2	**Prototype Timing System**
3	Specify
4	***PDR***
5	Modify specifications
6	Design TTCdec
7	Layout TTCdec
8	Manufacture TTCdec
9	Test TTCdec on DSS module
10	Design TCM
11	Layout TCM
12	Manufacture TCM
13	Timing system tests (TTCdec + TCM)
14	
15	**ROD Prototype**
16	***PDR***
17	Modify specifications
18	Design - JE/AS
19	Layout
20	Manufacture
21	Standalone tests
22	
23	**FPGA Programme**
24	Design Test module
25	Layout Test module
26	Manufacture Test module
27	***Ser- FPGA PDR***
28	Design Ser-FPGA firmware - IB
29	Test Ser-FPGA
30	Specify CP-FPGA - VP
31	***CP-FPGA PDR (Milestone)***
32	Design CP-FPGA firmware - JE
33	Test CP-FPGA
34	
35	**Prototype Backplane**
36	Specify interconnections
37	Specify electrical parameters
38	***PDR (Milestone)***
39	Design - O/M
40	Manufacture
41	Assemble and test in crate
42	
43	**CPM Prototype**
44	Specify - RS
45	***PDR (Milestone)***
46	Design - RS
47	Board layout
48	Manufacture
49	Standalone tests
50	
51	**CMM Prototype**
52	Specify - NG/VP
53	***PDR (Milestone)***
54	Design - VP/AS/KH
55	Board layout
56	Manufacture
57	Standalone tests
58	
59	***Prototype modules available (Milestone)***
60	
61	**Prototype CP System Tests**
62	
63	**Prototype "Slice" System Tests**
64	
65	***System Tests complete - PRR (Milestone)***
66	



Project: CPProject
Date: Wed 05-04-00

Task | Milestone | Rolled Up Split | External Tasks
Split | Summary | Rolled Up Milestone | Project Summary
Progress | Rolled Up Task | Rolled Up Progress