The ATLAS CPM Serialiser: Status Report

20-3-00.

- **Serialiser**
- **Serialiser Test Module**

Status: Serialiser

- Current design matches specification;
- Timing simulation completed successfully;
- Latency = 2 BC;
- Target device = XCV100E-6-PQ240
  - easier to achieve timing requirements with VirtexE rather than Virtex
  - Xilinx pushing users away from Virtex;
  - Production design: VirtexE or Spartan2 ?

- Serialiser pin out yet to be defined, but position of pins does not appear to be *critical* to performance in simulation.

Status: Test Board

3 FPGA designs completed:

Serialiser

- **the bit we want to test....**

SerialReceiver

- **looks like front end of CP chip:**
- **data synchronisation,**
- **serial-to-parallel conversion,**
- **BC DMUX,**
- **readout logic.**

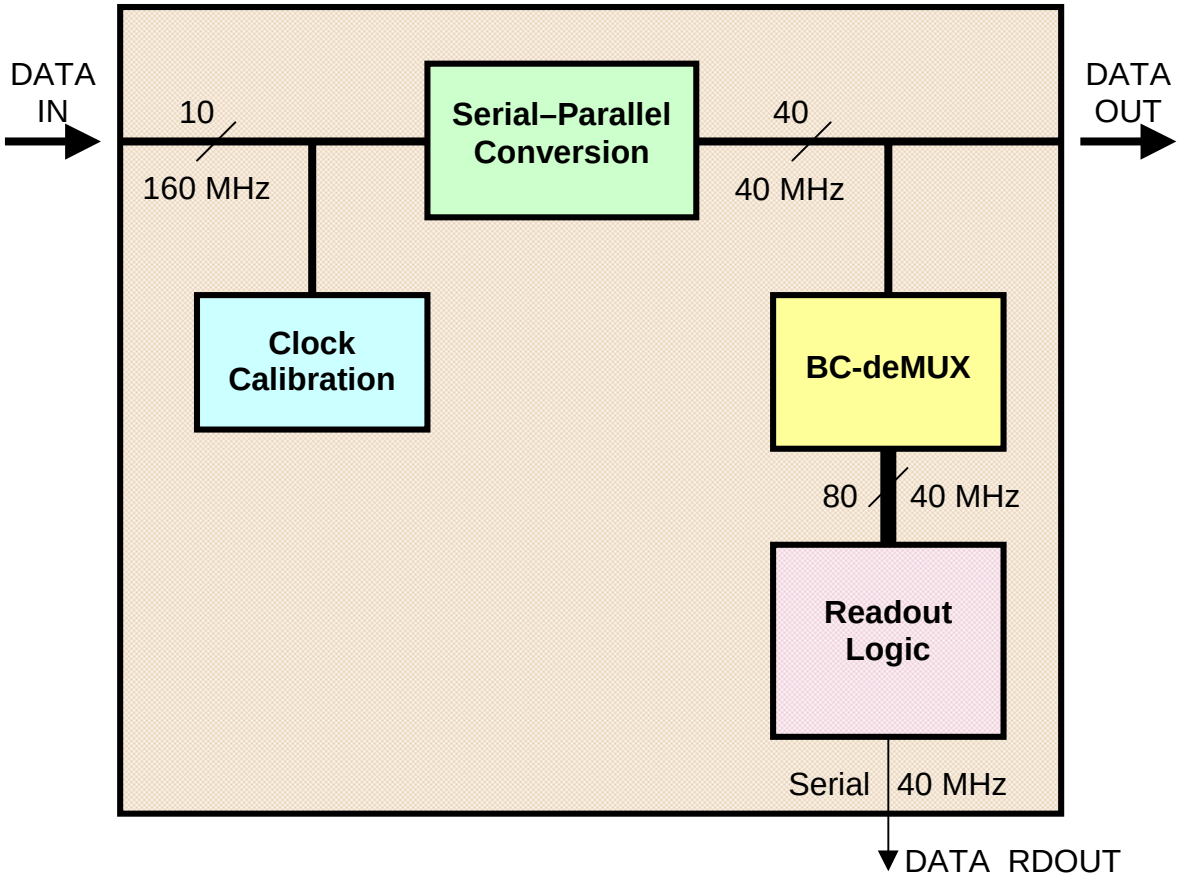
ROC

- **minimal read-out control...**
- **receives L1A**
- **generates all signals required to read out Serialiser (DAV, READ ADDRESS, etc)**

Serialiser Test Module — De-serialiser FPGA

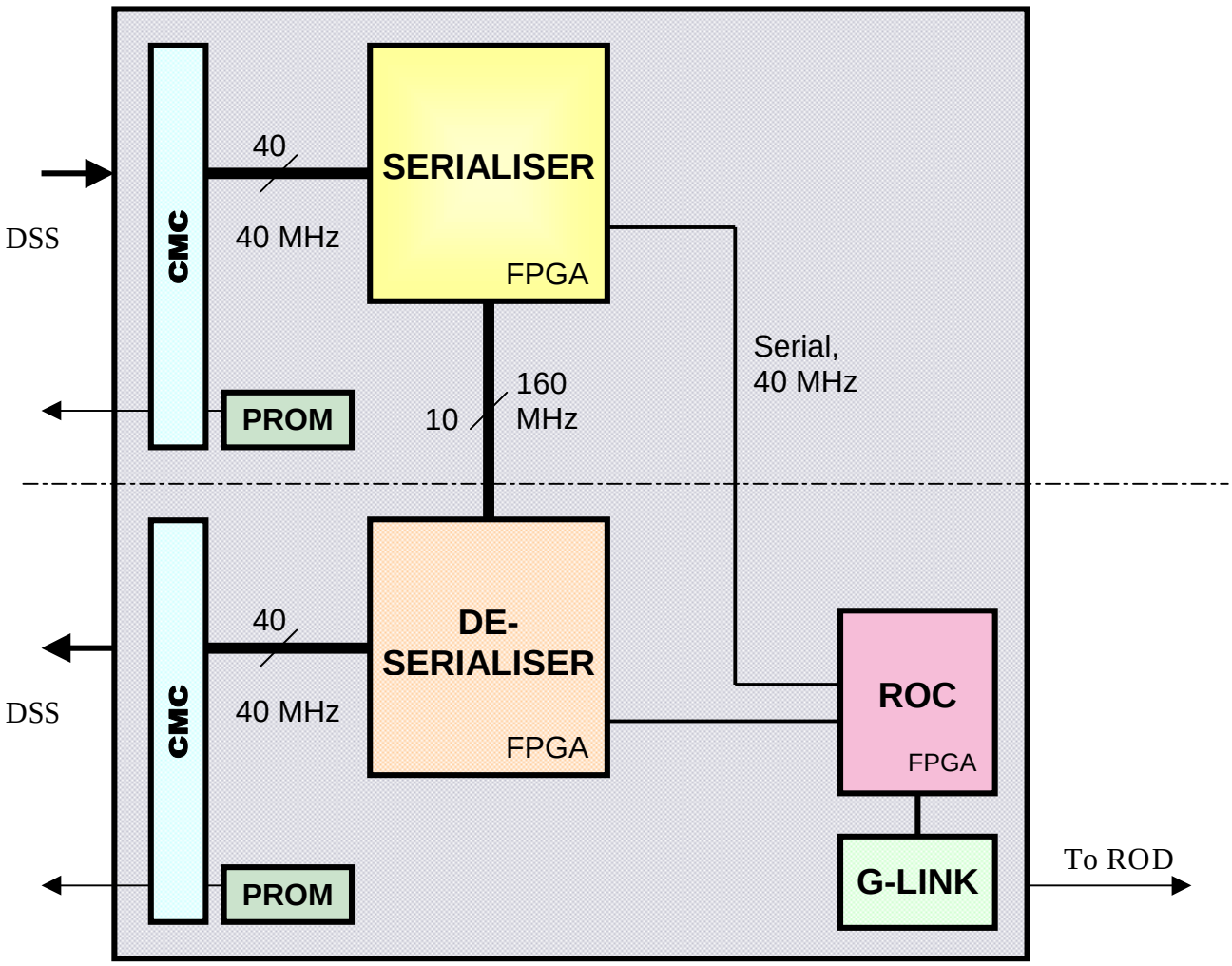
Looks like front-end of CP chip.

Design elements in Common with Serialiser, RAL215 ASIC and CP chip.



Serialiser Test Module — original proposal

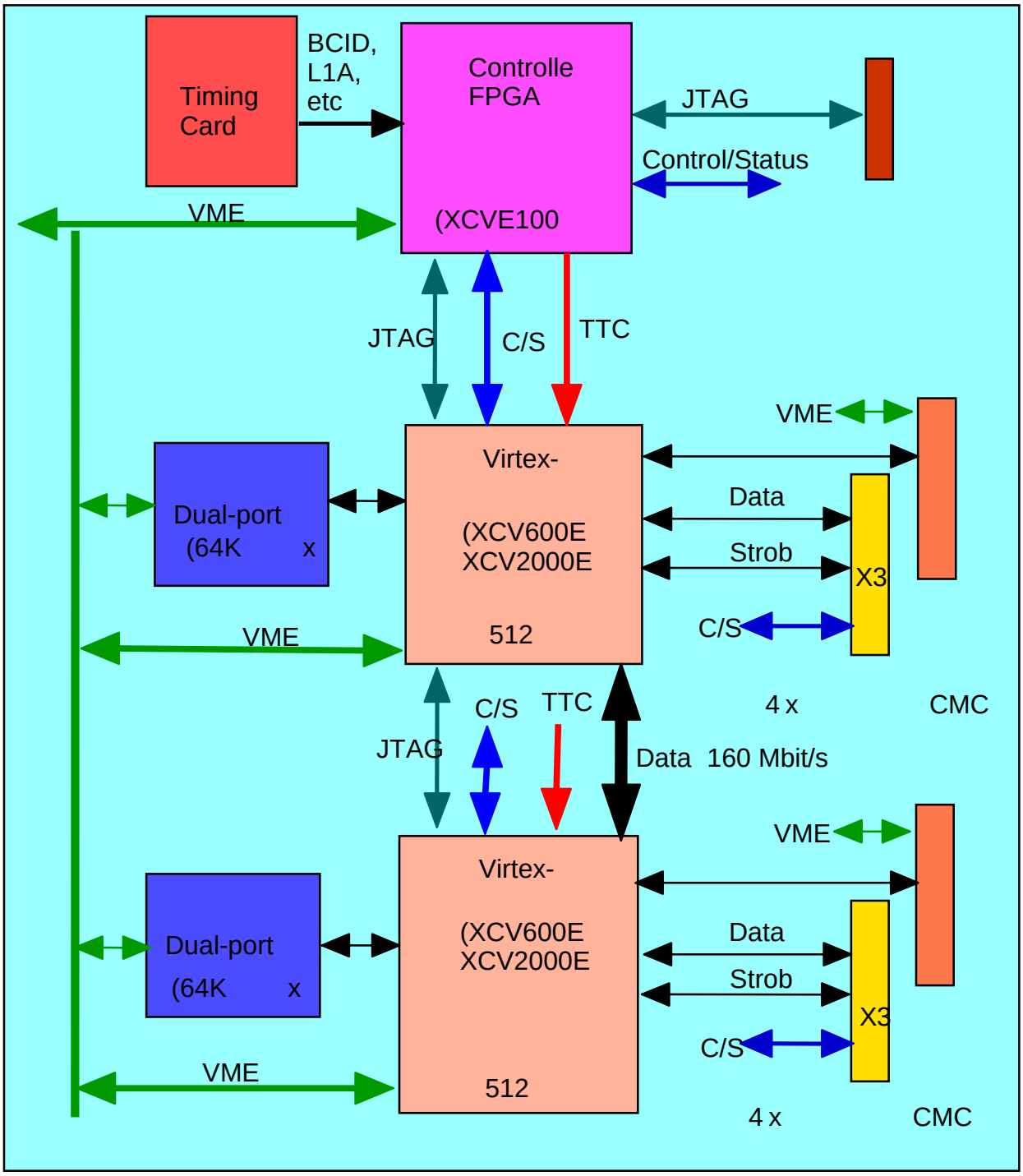
- **Double-CMC daughter board for DSS module.**
- **Motivation: test hardware implementation of...**
  - **— Serialiser**
  - **— *some* elements of CP chip**



Generic Test Module — new proposal

- Motherboard, 6U
- 2 CMC slots for daughter cards
- much of design common to DSS
- Dual-port RAM for data source and sink
- Direct VME access.
- Test hardware implementation of:
  - Serialiser
  - CP chip
- Share design effort with CMS
- Test Serialiser and CP chip in third quarter of 2000.
- For the Serialiser test, a device and package larger than that intended for the final system will be used, as...
  - we know from software results that design fits into required device (100k gates)
  - purpose of hardware test is to show that the algorithm runs @ 160 MHz in Xilinx of Virtex architecture.

Generic Test Module — new proposal



Summary

Aspects of Serialiser design which are not fully defined:

- **Device**
- **Package**
- **Pin-out**

Otherwise, bar changes in spec, design is finished.

Testing of Serialiser transferred from dedicated to generic module.

To be done: gain approval for, and fix specification of, generic module.