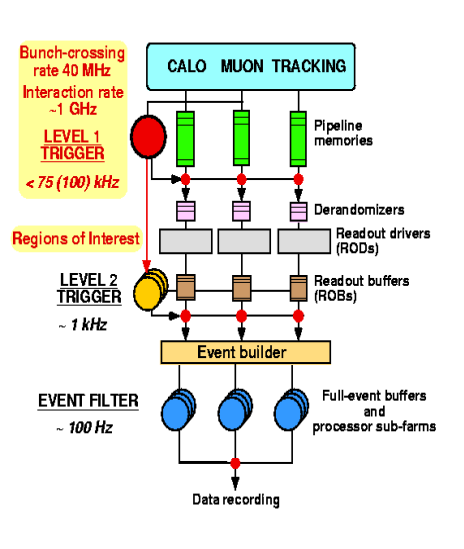
Level-1 Calorimeter Trigger

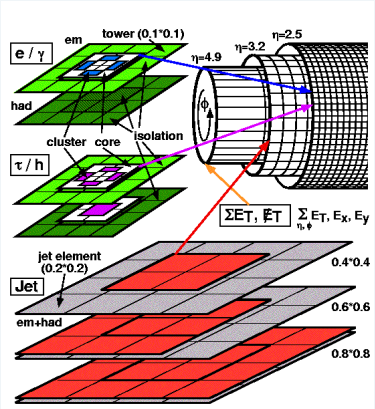
Queen Mary and Westfield College University of London, Rutherford Appleton Laboratory, University of Birmingham
University of Heidelberg, University of Mainz, University of Stockholm

ATLAS Trigger



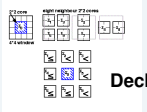
Trigger algorithms

- Cluster searches within parallel 4*4 sliding windows, over $|\eta|<2.5$.
- Isolated e/γ clusters in central 2*2 em core, with isolation vetoes in
  - em ring
  - had ring
  - had core
- Isolated τ/h clusters: e/γ clusters combined with 2*2 had core.
- Choice of jet cluster sizes: 0.4*0.4, 0.6*0.6 or 0.8*0.8, to tune noise rejection or efficiency, over $|\eta|<3.2$.
- Transverse energy sums -- ΣE_T and E_T^{miss} formed out to $|\eta|<4.9$.
- All features discriminated at 8 E_T thresholds --- 8 τ/h thresholds now e/γ or τ/h selectable.



Cluster, Jet and Energy-sum algorithms

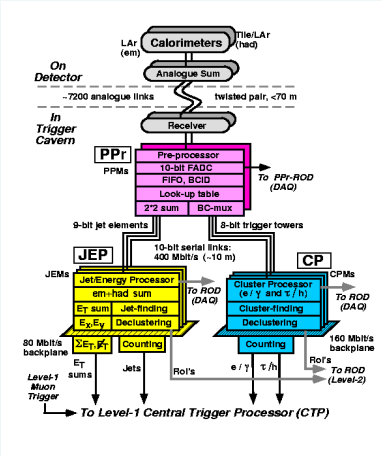
- RoI's are identified by *declustering* --- elimination of feature double-counting by windows in independent devices.
- New declustering algorithm is contained within a window and requires no additional hardware.



Declustering

Calorimeter Trigger Architecture

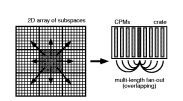
- Synchronous 40 MHz pipelined processor, identifying trigger features from 7000 calorimeter towers.
- Pre-processor: digitisation, BCID, noise suppression, calibration, jet input formation, multiplexing, error-encoding.
- 400 Mbit/s serial links to processors.
- Cluster Processor: serial link demultiplxing, 160Mbit/s backplane fan-out, e/γ and τ/h cluster-finding, discrimination, declustering, multiplicity merging.
- Jet/Energy-Sum Processor: link demultiplexing, E_x,E_y conversion, E_T summation, jet-finding,discrimination, declustering, merging.
- Feature multiplicities to CTP, RoI's to Level-2, inputs and results to DAQ.
- CP and JEP architectures converging, now sharing many common features and components.
- Birmingham responsible for CP module with strong involvement in all subsystems.



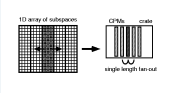
System	Item	Who	Description	Birmingham Contribution
Cluster Processor System	CP/JEP links	UK/Hdbg/ Mainz	400 Mbit/s LVDS links between PP and CP/JEP	Selected technology, designed test cards BER measured and error rate studied
	CP Module (CPM)	UK	Hosts CP links and CP chips, fan-out of trigger data, formats results, transmits to CMM and Level-2/DAQ	MAJOR RESPONSIBILITY Module design, manufacture, test CP system architecture
	CP chip	UK	FPGA/ASIC implementing e/γ/τ cluster-finding and RoI definition algorithms	MAJOR EFFORT e/γ/τ cluster-finding & RoI algorithms developed Design spec reviewed
	CP Serializer	UK	FPGA multiplexing link data to 160 Mbit/s for backplane fan-out	BC-multiplexing scheme refined Design spec reviewed
	CP backplane	UK	Fan-in/fan-out of data between CPMs Transmission of results to CMM	Fan-out topology proposed CPM connectivity defined
Pre-Processor System	PP-ASIC	Hdbg	Digitisation, synchronisation and calibration of input data	BCID algorithms developed and simulated; Design spec reviewed
	PP-MCM	Hdbg	Hosts FADC, PP-ASIC and LVDS links	Design spec reviewed
	PPP Module (PPM)	Hdbg	Converts analogue trigger towers to digitised trigger towers and jet elements	Calorimeter liaison
Jet/ Energy-sum System	JE Module (JEM)	Stock / Mainz	FPGA-based jet and energy-sum algorithms, transmits results to CMM and Level-2/DAQ	Jet algorithms developed and simulated Design spec to be reviewed
	JEP backplane	Stock / Mainz	Fan-in/fan-out of data between JEMs Transmission of results to CMM	Identical to CP backplane
Common Items	Timing/Control Module (TCM)	UK	Distributes TTC timing information used by PP/CP/JEP	
	Common Merger Module (CMM)	UK	Sums multiplicities of e/γ/τ clusters and jets Sums energy sum components -- used by CP/JEP	
	Read-out Driver (ROD)	UK	Formats DAQ/RoI data read from CPMs/JEMs used by CP/JEP	
	DAQ SW	UK	Level-1 control and dataflow within ATLAS	Code development
Tools	Data Source/Sink (DSS)	UK	Test platform for modules/components produced in UK	Daughtercards for LVDS test; Design spec reviewed
	Diagnostics	UK/Hdbg	Graphical access to HW programming model	First generation developed at Birmingham, second generation customized to UK modules

Components of the Level-1 Calorimeter Trigger and Birmingham's contributions.

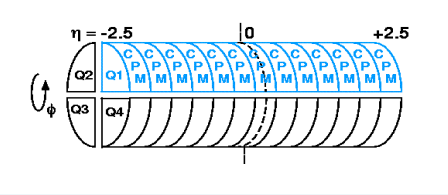
Cluster Processor Architecture



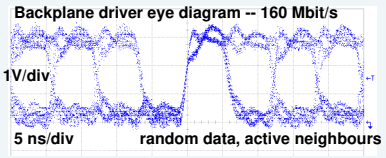
Demonstrator



Revised Architecture



- High-bandwidth fan-out to parallel processors is dominant challenge.
- Cluster Processor divided into quadrants in φ, one crate/quadrant.
- CP Modules (CPMs) map 1D array of sub-spaces --- logical partition matches physical implementation.
- CP backplane fan-out now nearest-neighbour only --- short signal paths with good isolation
- Multiplexing and error-detection across serial links and backplane.
- e/γ/τ multiplicities at 16 independent E_T thresholds go via backplane to Common Merger Module (CMM).
- CMM also used for jet and E_T sum merging ... master CMM merges crates and transmits results to CTP.
- Read-out of RoIs via 800 Mbit/s Glink to custom ROD; also used for DAQ read-out of inputs and results.

Cluster Processor Technologies

- 400 Mbit/s LVDS for PPr-CP/JEP links --- low power, BER < 10^{-13}.
- LV-CMOS backplane drivers demonstrated at 160 Mbit/s.
- 160 Mbit/s custom serialiser ASIC now to be implemented in FPGA.
- CP algorithm ASIC also likely to be FPGA implementation --- greater flexibility in refining algorithms.