Level-1 Co-ordinates

- Motivations
- Requirements and principles
- Systems and spaces
- CP labelling suggestions
- Conclusions

Motivations

- Several label formats have arisen (see PDRs)
- Conversions between labelling schemes
  - source of confusion and error
  - waste of mental energy (dominant in testbeam!)
- Implicit conventions to be defined and agreed
  - Obvious to everybody, but not necessarily in same way!
- Level-1 needs coherent labelling scheme
  - From calorimeter tower through to RoI
  - Covering towers/chips/modules/crates/systems
- Deliver
  - Coherent conventions for labelling signals and spaces
  - SW tool for translating/mapping

Requirements

- Comprehensible
  - Correspondence *to* system components
- Coherent
  - Correspondence *between* system components
- Efficient
  - Unique, consistent and duplication-free
- SW-usable
  - No fonts, special symbols or sub/superscripts

Systems and spaces

- Conventions should cover
  - Calo towers (cells?)*
  - Calo cables*
  - Receivers*
  - PPMs: PP-ASIC/MCM/Modules/Quadrants
  - PP-CP/JEP links
  - CPMs: CP-Serialiser/Chip/Modules/Quadrants
  - JEMs: Sum-FPGA/Jet-FPGA/Modules/Quadrants
  - Algorithm spaces (windows)
  - RoIs (*?)

  - = existing labels already defined

Principles

- Describe spaces by eta*phi*layer
  - Note window co-ordinates are (eta,phi)
- Start labels with 1, not zero
- Eta symmetry of space, but not of algorithms
  - But sequential module numbering hides inter-system module mapping, e.g. PPM-to-CPM
  - Use +/- eta symmetry in module labelling

    PPM(+/-n) => CPM(+/-n) and JEM(+/-n)
- Sequential quadrant labelling, Q1=0^{o}<phi<90^{o}

CP labelling (I)

- Algorithm space is 4*4*2 CP window
  - Inverse matrix notation, start at 1

4,1	4,2	4,3	4,4
3,1	3,2	3,3	3,4
2,1	2,2	2,3	2,4
1,1	1,2	1,3	1,4

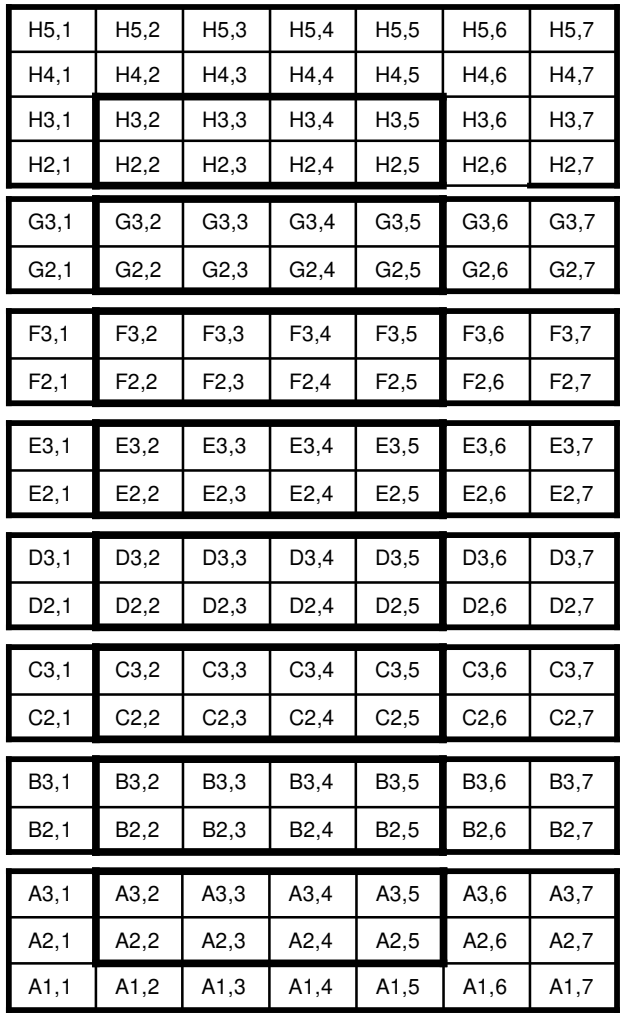
- CP chip co-ordinates as per PDR
  - Relate labelling of towers within chips and modules

5,1	5,2	5,3	5,4	5,5	5,6	5,7
4,1					4,6	4,7
3,1	3,2	3,3	3,4	3,5		3,7
2,1	2,2	2,3	2,4	2,5		2,7
1,1	1,2	1,3	1,4	1,5	1,6	1,7

- Label CP chips A-H,
- Reference towers as on-module co-ordinates

CP labelling (II)

- Label by CP-chip reference towers
- Inter-CPM fan-out simple…
  CPM_n(A2,4) => CPM_n+1(A2,1)
  CPM_n(A2,6) <= CPM_n+1(A2,2)
  CPM_n(A2,7) <= CPM_n+1(A2,3)
- Chips A and H *special*: environment rows A1,I H4,I and H5,I are inter-quadrant phi fan-out
- Serialiser: 4 BC-mux pairs *could* map CP-chip reference towers … serialiser => CP-chip map simplified



Conclusions

- Time for coherent Level-1 labelling scheme
- Implicit definitions should be made explicit
- Suggestions: CP towers labelled by CP-chip
  - Match Serialisers to CP-chip reference towers
- Consider other sub-systems on similar basis
- Tool for tracing signal names across systems
  - Web-accessible, DB-backed … Java?
- Level-1 proposal for Mainz …