Summary of Conclusions

- ***LVDS links:***
  - **Add low-jitter PLL to each Processor module —**
    - **→ to PPMs for stable LVDS links → CPMs/JEMs**
    - **→ to CPMs and JEMs for stable G-links → RODs**
  - **Two solutions to serial LVDS fan-out —**
    - **→ TI chip SN65LVDS104 (suggested by Richard)**
    - **→ HD designing 4-channel dual fan-out buffer ASIC**
- ***PPM "Module 0":***
  - **Evolve the PPM and associated backplane design to accommodate the TCM and TTCdec**
- ***Common Merger module:***
  - **Design to "Module 0" specification**
  - **Increase E-sum input B/W by use of bi-directional I/O**
  - **Draft specification available for discussion at Mainz meeting *(NG)***

- ***Prototype module specifications:***

  - **JEM and CPM prototype modules to be designed in 9U format to "Module 0" specifications and to use common backplane *(→ identical connector pin-out)***

  - **VME specifications to be defined by "VME Task Force" before Mainz meeting —**

    → minimal set of VME signals defined by NG + SS

    → 3.3V or 5V VME operation defined by VP + RS

  - **Use of latest AMP cable assemblies strongly encouraged *(low-smoke zero-halogen single-pair)* —**

    → explore cost, availability in different countries

    → build backplane space model to study connector insertion/removal problem *(tooling?)*

    → backplane pin-out to be re-defined by SS + RS

- ***Alternative front-end link architectures:***

  - **Virtex-E + Paroli has many attractive features, but —**

    → demands very low clock jitter

    → major impact on PPr MCM, compromise design

    → agreed to not proceed any further at present