CP ASIC/FPGA PDR — Summary

- **1-day review on Tuesday 25th January**

- ***Reviewers:*** **Paul Bright-Thomas**
  Ullrich Pfeiffer
  Sam Silverstein
  Richard Staley

- **E-mail comments from reviewers to Viraj in advance**

- **Viraj presented summary of the specifications and addressed major points from the reviewers**

- **A revised specifications document, incorporating most of the pre-review proposed changes, is already in preparation – draft available to reviewers**

- **List of recommendations discussed with Viraj at the end of the review**

Summary:

1. **<u>Error-monitoring</u> – concern about inability to identify rapidly which input channel is producing parity errors**
   - → ***add a 42-bit error register set by parity errors to indicate suspect channel***

2. **Saturation of digital sums**

   → ***specifications must define clearly how digital arithmetic treats saturation***

3. **Isolation thresholds**

   → ***include logic to ensure that setting isolation threshold to FF is equivalent to turning isolation off***

4. **FIFO control**

   → ***add input signal ("FIFO flush") to empty FIFO on demand from CPM Read-out Controller (to guarantee correct shadowing of ROC FIFO)***

5. **Unused inputs – it is essential that where serial inputs are not driven *(e.g. at η extremes)* their data are set to zero, but this would generate permanent parity errors**

   → ***add a mask register to disable parity-checking for unused channels***

   → ***confirm that the Serialising FPGA sends all-zero bitstreams when fed from a non-driven LVDS Rx***

6. **Input data monitoring – considerable concern expressed about difficulty of monitoring incoming data only via scan path technique**

   → ***explore alternative techniques – e.g. by loading new configuration file into chip (only if FPGA)***

7. <u>ASIC *vs* FPGA</u>

→ ***include some indications in the specifications about the criteria for choosing between ASIC or FPGA implementations (latency-cost trade-off, etc.)***

8. <u>Schedule issues</u>

→ ***specifications must include details of how the CP ASIC/FPGA design-manufacture-test schedule meshes with the similar schedules for the Serialising FPGA and CPM prototype***

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Conclusions from the two reviews:

- ❑ **Combining pre-review written comments (via e-mail) with a full 1-day meeting was very successful**
- ❑ **This was a much more effective way of reviewing designs that was used last year *(e-mail alone)***
- ❑ **Most valuable feature was the dialogue between reviewers and designer(s)**
- ❑ **Several points emerged which had not previously been noticed, only because of the interaction of discussions**
- ❑ **This will serve as a model for all future reviews**