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- **Summary of Test Results**
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Summary of Test Results

LVDS Links Operating with error rates < 10^{-12}, over 10m and 15m cable lengths.
Most Links are giving < 10^{-13}.

Using 4 pair cable from Datwyler, with matching pre-compensation LR circuit.
(Tolerance +/- 2m)

Have achieved errors rates of 10^{-12} over a single 20m cable.

A low level error rate still present, even after attention to LVDS circuits. Re-design of PCB needed to give quieter supplies.

No noticeable increase in error rates observed even with

- Source and Sink in separate crates.
- Continuous VME reads from Sink DSS.

Comments

Errors appear timing related, due to poor jitter tolerance of LVDS receiver.
Manufacturer's Spec gives 100ps jitter tolerance guaranteed, with typical devices toterating 400ps.

Timing Jitter caused by

- Noise on supply to LVDS transmitter affecting PLL
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- Cable integration (reduced by equalisers)
- Quality of applied Clock. ->

Next

- Tests with TTC . Very important

- New LVDS Sink card
  (with filtered supply for LVDS Rx)
  RAL Drawing Office have finished layout.
  2 assembled PCBs requested.

- Another version of LVDS Sink card with long PCB tracks ?

- LVDS Source card to be re-designed.

- National have a faster LVDS device in development. 40MHz to 66MHz. Watch the Web!