PPr MCM PDR — Summary

- **1-day review on Monday 24th January**

- ***Reviewers:*** **Christian Bohm**
  Paul Bright-Thomas
  Viraj Perera
  Uli Schaefer

- **E-mail comments from reviewers to Ullrich in advance**

- **Ullrich presented summary of the specifications and addressed major points from the reviewers**

- **List of recommendations discussed with Ullrich at the end of the review**

Summary:

1. **<u>Analogue input network</u> – must not use input resistance of FADC chip to control attenuation – uncertain by >10%**

   → ***redefine circuit to give precision <1%***

2. **<u>PHOS4 timing chip</u> – momentary interruption of clock corrupts stored timing data, resettable only by power-down/up**

   → ***investigate failure modes urgently and explore possible monitoring procedures***

3. **<u>Effect of clock jitter on LVDS Tx</u> – TTC specifications show maximum jitter > LVDS Tx requirements, possibly increasing link BERs**

   → ***repeat LVDS link tests using TTC system***

   → ***investigate possible use of new faster NS LVDS serialiser-deserialiser chipset***

   → ***consider use of "repeater" PLL with long time-constant on PPM to feed LVDS Tx chips on MCM***

4. **<u>MCM manufacture</u>**

   → ***include more detail in the specifications about the precise sequence of manufacturing steps***

5. **<u>FADC chip</u>**

   → ***justify in the specifications the choice of FADC device***

6. **<u>Use of G-links</u> – if LVDS were to run into serious problems, our only fall-back link possibility is G-link, but this would have major consequences**

   → ***outline in the specifications what the implications would be for the MCM design***

7. **<u>LVDS Tx operation</u>**

   → ***specify 100 ohm MCM trace impedance for differential LVDS bitstream signals***

   → ***specify clearly the power supply decoupling to be provided for the Tx dies***

8. **Pre-compensation and fan-out**

   → ***chosen technique for LVDS fan-out and cable pre-compensation must be thoroughly tested before final MCM design is frozen***

9. **Schedule issues**

   → ***specifications must include details of how the MCM design-manufacture-test schedule meshes with the similar schedules for the PPr ASIC and PPM***