Serialiser Status Report,

Ian Brawn, 31-1-00

Serialiser:

- design matches specification.
- Timing simulation completed OK.
- Pin out to be defined.

Test Module:

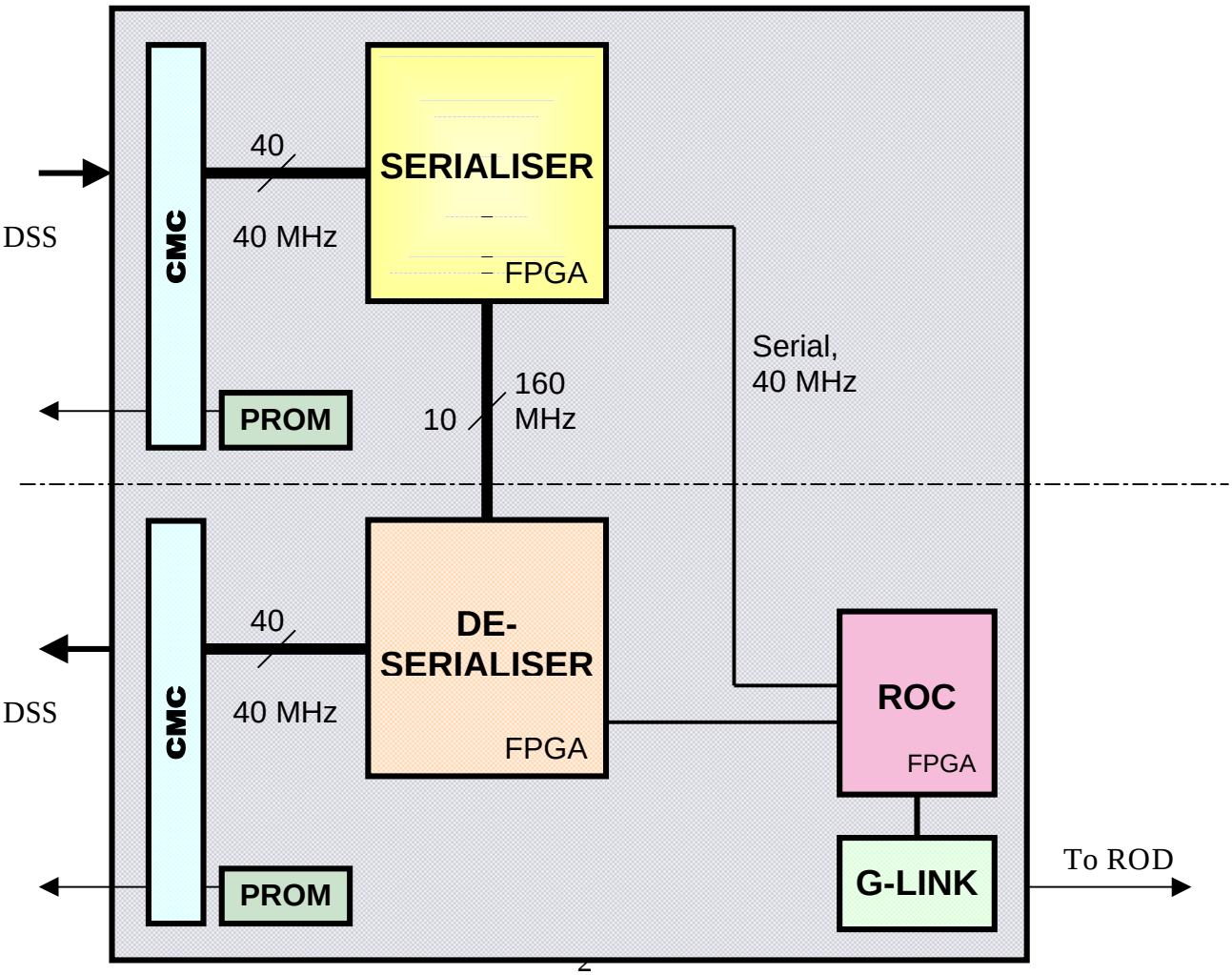
- Design of SerialReceiver underway:
- FPGA design targeting VirtexE device.
- Initial design complete.
- functional simulation completed OK.
- Next: synthesise, target device and simulate timing.

Serialiser Test Module

Double-CMC daughter board for DSS module.

Motivation:

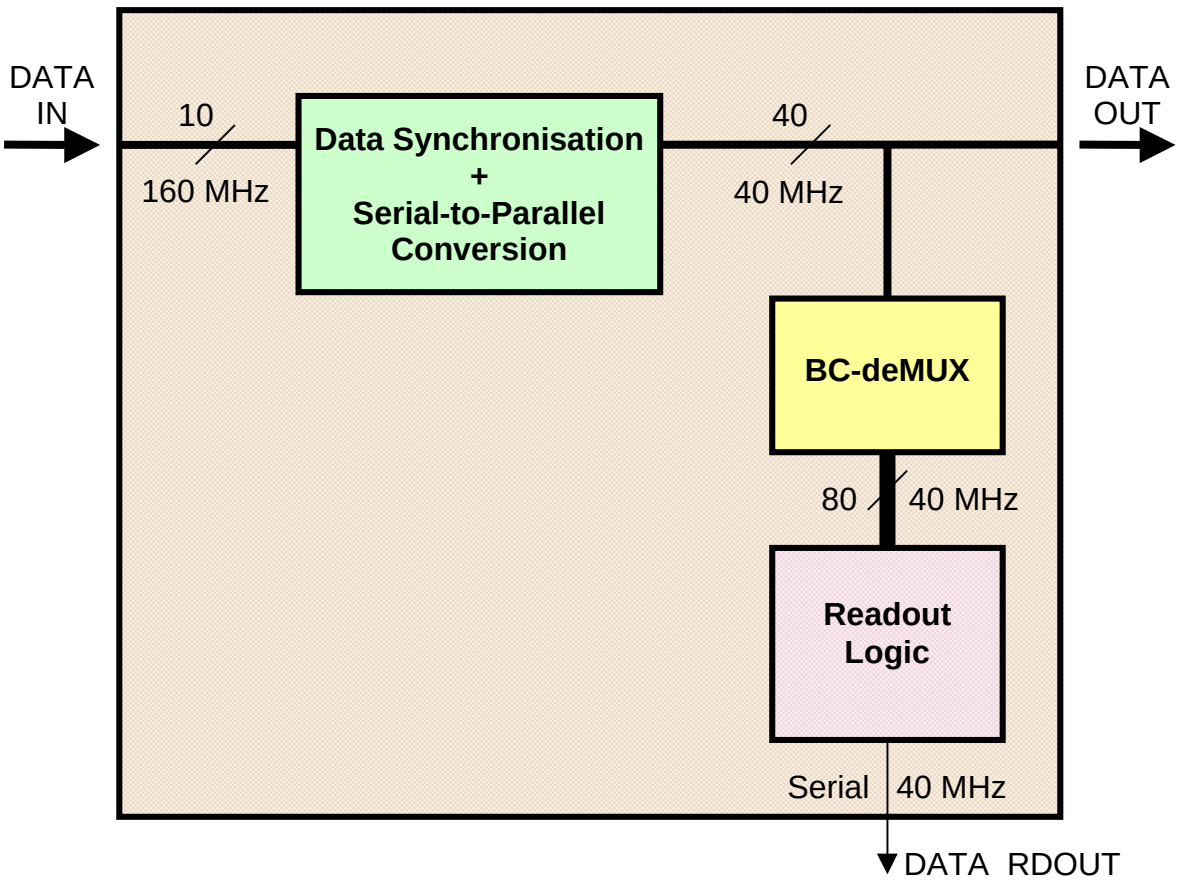
- test hardware implementation of Serialiser:
  - real-time path;
  - readout path.
- Test some elements of CP chip.
- Possibly provide data source for ROD tests.



Serialiser Test Module — De-serialiser FPGA

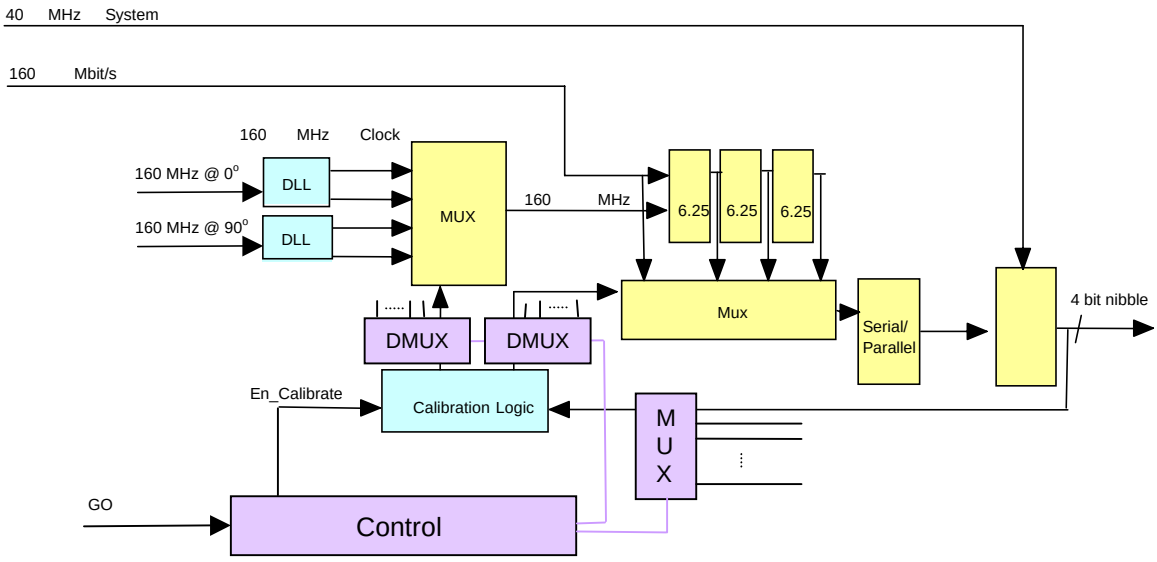
Looks like front-end of CP chip.

Design elements in Common with Serialiser, RAL215 ASIC and CP chip.



Synchronisation, S-to-P logic

- **Logic based on RAL215;**
- **expanded from 1 serial channel to 10 channels with independant timing.**



10 instances required (RAL215)

1 instance required (RAL215)

1 instance required (new logic)