ATLAS Level-1 Calorimeter Trigger
Hardware Progress Meeting – 8 May 2001

Minutes

Present: Stephen Hillier, Gilles Mahout, Richard Staley, Bruce Barnett, Norman Gee, Viraj Perera, Ian Brawn, Bob Hatley, Eric Eisenhandler (chair and minutes)

1. Generic Test Module: Viraj

Components and PCBs are now ordered for new batch; delivery expected in about four weeks and should be assembled within about five weeks from now. Non-working re-worked module has not come back and nothing yet about who pays. It will be sent to another company that has been found with a machine for re-working, together with the 'engineering sample' Xilinx XCV600 chips (see DSS saga) — this will serve as a test of the new company.

2. CP FPGA: Ian

James is currently doing simulations. The main issues are discussed separately in items 4 and 5.

3. CPM: Richard

Three more schematics have been completed, but there is still about two weeks work before the schematic review can be held. Main outstanding item is readout controller, which has lots of detail but no obvious showstoppers. Gilles has designed this, but needs to simulate it and then decide which Xilinx chip to use. Norman was assured that all FPGAs used on the board will have ample spare capacity for future developments. Also see item 5.

4. How many CP FPGAs to order: Discussion

Should we fully populate all four CPMs with CP FPGAs, and when should we buy them, since they are very expensive but the price might come down at any time. First comment is that nothing will be wasted since all chips should be usable in final boards, but we might be paying too much . Second comment is that the chips in the CMM are not the same, despite family name, since the package is different. So minimum number needed in order to include tests of inter-crate merging is $1\times8 + 3\times3$; maximum number is 32.

There was general agreement that we should not cut corners, and aim to populate all four boards fully. This might not be done initially but we should have enough chips to do it when we decide to. The first board to be built *must* be fully populated to test it properly, and doing that in stages would waste precious time so it should have all FPGAs from the outset.

When to buy? It might be four months before we have any boards, and FPGA delivery is claimed to be 6–8 weeks. We decided to order 8 FPGAs right away, to be absolutely sure that testing of first CPM is not delayed by lack of chips, but to wait about two months before ordering a further 24 in order to benefit if there is a price reduction. However, the distributor should be checked periodically to see if FPGA delivery times have changed, and if delivery times worsen we should order the rest of the chips sooner.

5. CPM vs. CP FPGA tower mapping?

Ian's examination of Steve's test vectors had revealed a serious inconsistency between the CPM specification and the CP FPGA specification and firmware. The problem is basically that the CP FPGA has to handle five ϕ bins in order to fully process two ϕ bins, but due to b.c. MUX it actually takes in six bins. The misunderstanding is over whether the bin at the high or low ϕ end is ignored: in the FPGA firmware it is assumed that the high bin is ignored, but the CPM specification assumes it is the low bin. Neither specification is very clear or explicit about this, and logically either one is usable so correcting things could go either way. However, there are various implications: re-writing the firmware would take a lot of effort and might be error-prone, also we need to understand what the boundaries of the CPM's "phi quadrants" really are (not multiples of 90°?), and in addition we might have the awkward situation of RoIs and hits sometimes reading out from different CPMs (this needs to be checked). This did not seem like a decision we could take on the spot, so people were urged to go away and carefully think through implications, and also to evaluate how much work it would be to change the FPGA firmware since it is probably better to use the CPM scheme since it seems a bit more logical and intuitive. An attempt to make a firmer decision should be made at the next hardware meeting. (Note: it is believed that the JEM will not have this problem since there is no b.c. MUX, but this should also be checked.)

This is an illustration of the usefulness of test vectors devised by someone who is not involved in the design. A discussion on how thoroughly the CPM could be simulated in VHDL, and the implications in terms of using up precious effort, concluded that there might be some time to look at things like this while modules are in the drawing office.

6. TCM and Adapter Link Card: Bob

The TCM and ALC were ready to go out to manufacture (7 TCMs and 6 ALCs), but it was discovered that the power sockets specified are now obsolete. A substitute is being sought, and manufacture is being held in case this requires changes to the layout.

It is not clear what has been done for the JEM, which has the same problem unless Uli has found a supply of the specified sockets. Bob will contact Uli to find out what he is doing about this.

7. CPU Personality Card: Bob

The design has gone to the RAL drawing office, but layout has not yet started. Bob is designing the metalwork for it. A newer CPU model is now being ordered; it should not be different in terms of the Personality Card but since it has IDE rather than SCSI Norman will double-check its through-pin requirements.

8. CMM: Ian/Norman

Work on the design is progressing and it should be ready for layout in about two weeks. Ian has found a source of LVDS transceivers to use. Norman has produced version 1.0 of the specification and it is now signed off and will be put into EDMS.

The parallel LVDS daughter card needed to test the CMM with the DSS has been specified by Viraj. A simple and nearly passive stub board to check backplane continuity will also be needed.

9. AOB

Bob has received the metal for the power supply assemblies, but the psu's themselves have not yet arrived. He will start to assemble it.

The **next meeting** is on 22 May at 14.00 in RAL CR1.