ATLAS Level-1 Calorimeter Trigger
Hardware Progress Meeting – 22nd May 2001

Minutes

Present: Bruce Barnett, Eric Eisenhandler, Norman Gee, Tony Gillman, Steve Hillier, Viraj Perera

1. Update from Heidelberg, Mainz and Stockholm

Tony summarised briefly the status of hardware development at the three non-UK institutes, following e-mails from Uli and Sten.
The Heidelberg status can be found in the minutes of their weekly (Wednesday) meetings at http://wwwasic.kip.uni-heidelberg.de/atlas/L1/HD_MEET/.
In Mainz, there is a continuing problem with the JEM prototype, where the Spartan II chips were assembled rotated by 180 degrees. The assembly company is confident that re-work will be feasible (vapour-phase technology), but there are plenty of spare chips if necessary. As there are known pcb bugs, and also some concerns about selecting the correct values for back-termination resistors, it may be preferable to re-design the board now and test the new iteration. This will be discussed further. The JEM programming model has been updated (and approved by Murrough).
(N.B. In general, Uli would welcome sharing more frequent discussions with us at our hardware meetings, either by coming along in person or joining in via a video/audio conference link.)
In Stockholm, the call for Backplane tenders closes on June 4th, so no more news until then, after which time we can re-assess the schedule.

2. CP FPGA

Viraj reported that James is finding that the firmware synthesis takes about 36 hours, even on a fast PC with a lot of memory. Running on a Sun will be explored (file format compatibility?), as this is looking uncomfortably slow. A standard pitch BGA package will be targeted (BG560 – 560-pin device – £580 each), as the fine pitch packaging is not required (and would probably also make re-work more difficult). Eight chips will be ordered immediately (4-6 weeks delivery) for the first complete CPM, with further devices to follow later, hopefully benefiting from a price reduction.
There was further discussion about the tower mapping from CPM into the algorithm on the CP FPA (see minutes of last meeting). It was decided that when Ian returns from vacation he should assess the difficulty of changing the mapping between the deserialiser block and the algorithm block to ignore the low-phi row (rather than the high-phi row), and if reasonably straightforward this change should be made now.
It was also agreed that Steve would check that the tower mapping (and notation) was consistent throughout the processor signal chain, from Pre-Processor to CP FPGA algorithm functional block.

3. Generic Test module (GTM)

Viraj reported that new boards and component sets for two new modules had been ordered, with assembled modules being available by mid-June. He added that SDI have “lost” our re-worked board – hopefully only temporarily! He has found another company offering re-work capability (Cemgraft), which has already successfully re-worked one of the DSS modules, which we will ask to try and re-work the GTM (if it is ever re-discovered!).

4. Parallel LVDS transceiver CMC
Viraj reported that Adam Davis has finished the schematics, and the design is almost ready to go into the Drawing Office for layout.

5. TCM + ALC
In Bob's absence, Tony reported that manufacture of the TCM and ALC is still on hold, awaiting a guaranteed supply of AMP-like affordable power pins from Siemens. The distributor is working on the problem.

6. CPU Personality Card (CPC)
Norman outlined the problem of hard disk usage with the Concurrent CPU modules. The executive summary of the proposed solution is that we proceed with the existing CPC design unchanged (currently on hold in the Drawing Office), mounting the hard disk locally on the inner side of the 9U crate side-wall to keep the total length of the EIDE bus below 17 inches. Dedicated 5V and 12V supplies will be provided via flying leads.
If in the future we wish to use a CPU-mounted PMC board requiring 12V this would not be possible, as our VME-- does not provide this voltage rail. When Bob returns, he should check if it is simple to provide an on-board 1A 12V DC-DC converter on the CPC before the final layout starts.
There was some lengthy discussion about testing the TCM/ALC/CPC boards, in the absence of the PB. It was suggested that if the Heidelberg ALC were available it could be used to test the TCM in any 9U crate fitted with a standard VME J1 bus. To test the ALC and CPC boards, a "stub" backplane interfacing VME-- to standard VME would be needed. Steve will check if Simon could design this at Birmingham. It was generally agreed that a clear plan should be developed for all pre-PB module testing.

7. CPM
Tony summarised the CPM status, following Richard's and Gilles' e-mails:

- The TTCrx controller FPGA has been packaged and is on the schematics.
- A PLD to drive the front panel LEDs has been added, stretching the indication where necessary. This is now on the schematics, and the packaging is nearly complete.
- The schematics sheets have progressed as follows:
  - TTC + clock distribution (sheet 6) is near completion
  - Serialiser readout connections (sheets 26 and 27) are complete
  - Indicators (sheet 35) are near completion
  - CAN controller (sheet 38) is complete
  - Much work is still to be done on the Readout Controller and Hit logic schematics (sheets 28 and 29) and the backplane connectors (sheets 39 and 40)
  - JTAG chain (sheet 37) needs some attention

- The CPM Memory Map document has been updated and is now on the web at: http://www.ep.ph.bham.ac.uk/user/staley/cpm_memory_map.pdf
- The Serialiser addresses have now been corrected from those given in the PDR specification, amongst other changes

- Gilles has been making good progress on the XILINX ROC designs, with successful functional simulations, and parts now need to be packaged to complete the schematics

There is no further update available on the date for the schematics review, but it is probably at least another two weeks away.

8. CMM
Norman noted that all HIT signal I/O would now use 68-pin SCSI connectors.
Viraj reported that the CMM schematics were complete and had been independently reviewed in his group. The final version (1.0) of the specifications, together with the schematics, will be posted on the web next week, at which time comments from Uli and Sam will be invited before the design goes to the drawing Office for layout.
Tony will request mechanical dimensioning details of the backplane from Sam.

9. FPGA firmware maintenance
There was some discussion about FPGA support, now that so much of the system will be dependent on a large amount of complex firmware. It was agreed that each designer must have some form of backup by another engineer, who would understand their design sufficiently to make changes efficiently.
This issue will be addressed further at the Mainz Joint Meeting.

10. *AOB*
By this time (16:40), fortunately there was none.

Next meeting - Tuesday 12th June at 14.00 in CR01, R1 at RAL. Refreshments will be provided.