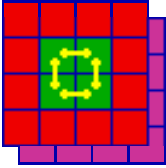


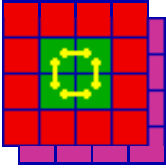
## ***Highlights and lowlights: RAL, 8–10 November 2001***

- ◆ Personal view, **not** a comprehensive summary of all that was presented and discussed.
- ◆ Apologies for anything important that's missed (**tell me**).
- ◆ If you think anything is mistaken or objectionable please say so!
  
- ◆ The categories are as follows:
  - + a positive, or mainly positive, development, or something that has been sorted out, or simply good progress.
  - a negative development, or something that needs to be sorted out that may cause problems, or an item where work seems to have stopped — no criticism of people involved is (necessarily) implied.
    - ◆ more work or a decision is needed.
    - ! a controversial point that must be discussed further.
- ◆ No names mentioned since it's very difficult to be fair to everyone who has done all the work — people will know who they are!



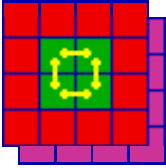
# ***Calorimeter signals and cables***

- + **Nice thorough job done on compiling signals from calorimeters — a few questions but mostly they seem o.k.**
- **Who builds receivers (TileCal and even LAr) still not defined, but we will know about LAr (and maybe even TileCal) soon**
- **TileCal cable situation messy**
- **Rack layout situation still not entirely clear (use of middle hole, position of CTP, wall); must also consider front-of-rack cabling**
- ◆ **Must document in detail connections from calorimeters to Preprocessor**
- ◆ **This includes checking/specifying of all receiver interconnect boards**



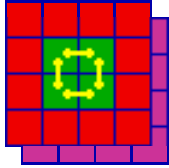
# *Preprocessor*

- + **Steady progress on ASIC, almost ready to send it out**
- + **None of the problems found affect real-time data path**
- + **Can now use high-speed LVDS dies on MCM**
- + **First MCMs built (except for ASICs)**
- + **Good planning for tests**
- + **PPM making good progress, including AnIn**
- + **Test plans made for quickly evaluating ASIC and MCM**
- + **Readout and ROD progressing**
- + **New and better estimates of rates and compression**
- **But we said that at the last meeting!**
- **But looks as if ROD needs two S-links to read out even 1 BCID + 3 raw data slices, and can't do 1 + 5 at full speed**
- ◆ **Much documentation still needs updating (also said at last meeting)**
- ◆ **Think about the synchronisation requirements and implementation for analogue inputs from video memories**



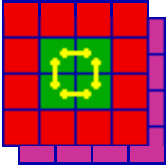
## ***CPM and JEM***

- + **CP FPGA tests progressing well**
- + **CPM being laid out**
- + **Work on JEM firmware has resumed**
- + **New work on jet algorithm firmware**
- **CPM timetable slipped, on critical path**
- **Long sad saga of first JEM prototype**
- **Still production problems to get another one made**
- **How to proceed to a completely full-specification prototype still not clear**
- **Might only test full-spec module in phase 2 of slice tests**
- ◆ **JEM documentation still needs updating (also said at last meeting)**
- ◆ **Pick up on PCB design points for easier reworking**
- ◆ **Online software work needed**



## ***Common modules and backplane***

- + **CMM nearly ready to send out for manufacture**
- + **TCM and adapter link card progressing well**
- + **Backplane almost ready to go, various small problems solved and manufacturer has helped a lot**
- + **Further progress on debugging CP/JEP ROD prototype**
- + **Route cards and problem reports introduced to document individual faults and general problems**
- **CMM, CPM, TCM somehow used wrong front panel specification!**
- **Backplane timetable slipped, on critical path**
- ◆ **CMM will give us important information on the feasibility of 9U boards with fine-pitch BGAs**
- ◆ **Decide how many TCMs to assemble; use current layout**
- ◆ **Backplane documentation should be finalised**

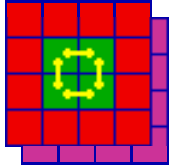


# DCS

+ **Progress on Fujitsu local DCS solution for modules**

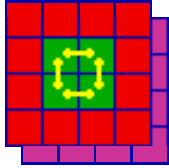
– **Fujitsu support is poor, probably not the best choice for ‘cut-down’ solution**

- ◆ **Should finish getting demonstrator system working and reading out real voltages and temperatures on TCM**
- ◆ **Better choices for on-board chips seem to exist, and others may be coming**
- ! **Possibly use ELMB on TCM as bridge between crate CANbus and outside world**
- ! **May have to add a second CANbus interface to ELMB (e.g. via SPI)**
- ! **Could still decide in final system not to monitor each module**



# *Physics simulation*

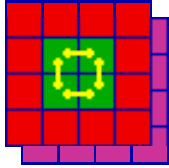
- + **Work progressing on trigger simulation**
- + **Now working with CTP on trigger menus**
- + **Birmingham funded to build big new PC cluster for simulation**
- **ATHENA installation and documentation situation (especially for people not at CERN) is appalling**
- ◆ **Need to finish jet and  $E_T$  algorithms**
- ◆ **Need to add features such as thresholds varying with location**



# Online software

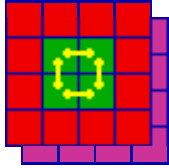
- + **Much progress in defining packages and saying who is responsible for developing them**
- + **Progress on run control, databases, simulation, modules, ...**
- + **Balanced view of the future role of HDMC emerging**
- **Want a standard, well-described distribution of software for ROS!**
- **Want ROS/ROBIN configuration to stabilise and stop changing every time we ask about it!**
- **Still have shortage of effort to develop software and firmware, and to test modules — but new people at Mainz and Heidelberg**
- ◆ **Large number of documents to finish (e.g. requirements), so decide which ones really need full review procedure and concentrate on them**
- ◆ **Debugging complex firmware will not be easy!**
- ◆ **Remove ‘barrier’ between firmware engineer and test-vector authors**
- ! **Try to get non-software experts to do as much module testing as possible (said this last time)**





## ***Slice test and timescales***

- + **We have made a lot of progress, and modules are now about to be manufactured**
- **Commissioning/testing phase will be complex and it is very difficult to predict duration (yes, we said that last time)**
- **DIG must tell us whether we should use ROS or ROD-crate DAQ, and on what timescale**
- **Slice test now end June at earliest**
- **We are not good at estimating timescales, and module commissioning time is very hard to predict**
- ◆ **Must not send modules for slice test until they are working well on their own *and* in their own subsystem**
- ◆ **Need user guides as well as up-to-date specifications for all modules**
- ◆ **Should write test plans as early as possible**



# Summary

- + **There has been a great deal of progress!**
- + **Try to use regular, short telephone conferences to keep groups informed about status**
- + **Think a bit about possible showstoppers and how we might react to them**
- **... But also slips in timescale, shortage of effort**
- ◆ **Do not neglect documentation; we already have problems of lack of continuity as people leave and are replaced**
- ! **Power-cut note: slides are less necessary than we think, and do not stop the ‘show’!**

**Thank you to the RAL group for a productive, well-organised meeting in pleasant surroundings!**

**Special thanks to Norman for dealing with the accommodation nightmare!**