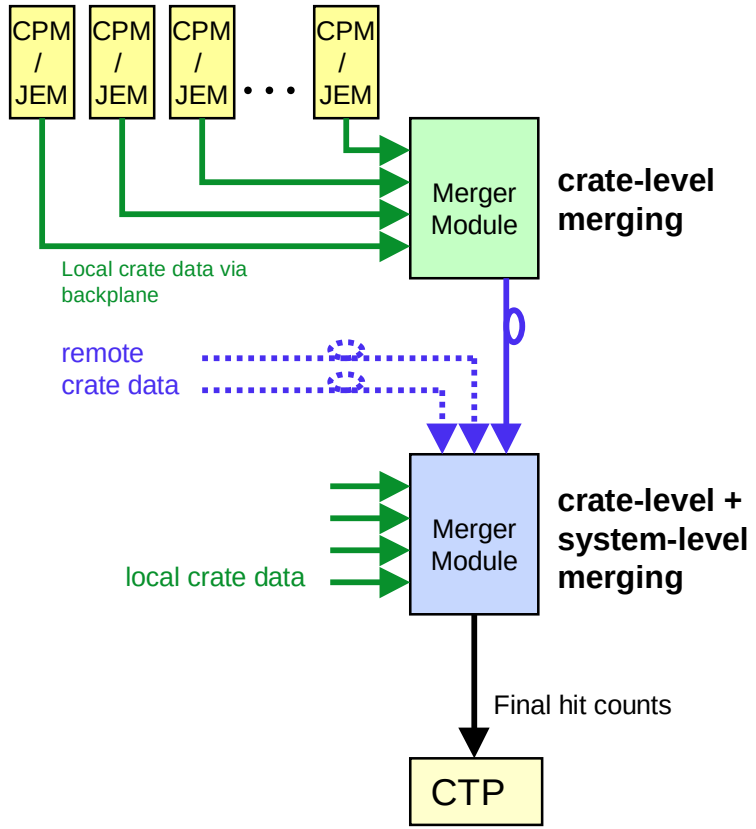
The Common Merger Module, Rear Transition Module & cables: Status and Schedule

- CMM Design Overview
- The Rear Transition Module
- Cables….
- Current Status
- Schedule

Design Team

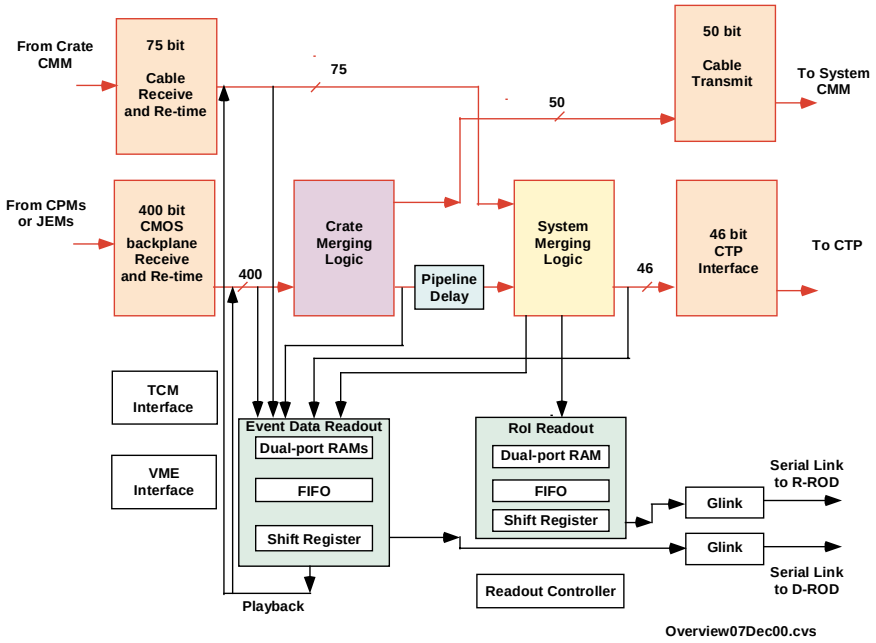
- Viraj Perera - project manager
- Panagiotis Apostologlou - schematic entry
- Ian Brawn - firmware
- Dan Beckett - layout

CMM Overview



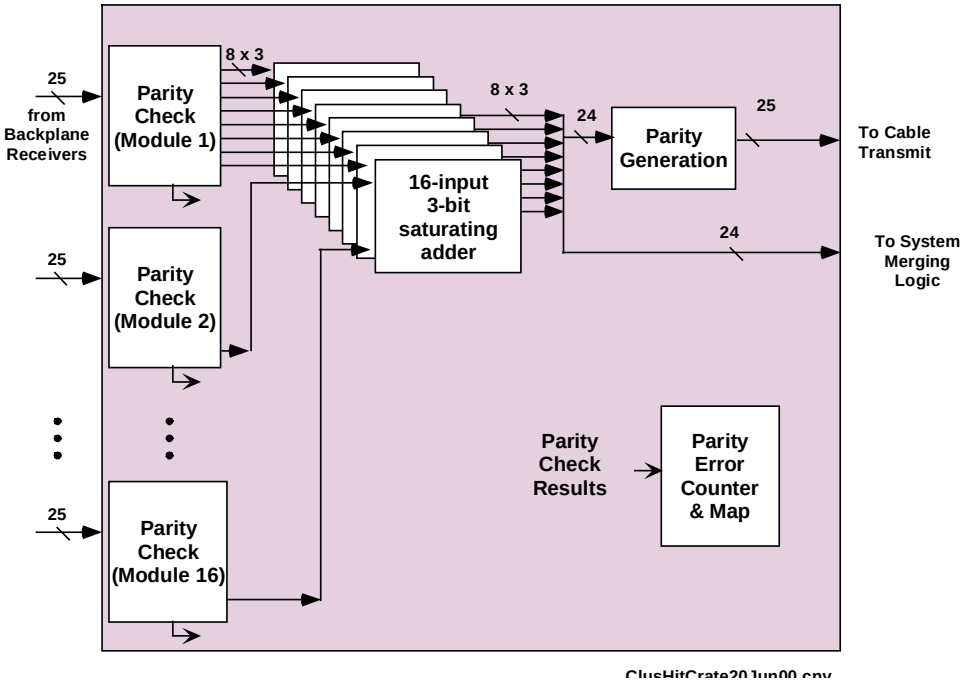
- CMM = multi-purpose module used in CP and JEP subsystems to merge
  - e/γ & τ hit data
  - Jet hit data
  - Energy data
- Type of data-merging performed determined by configuration of on-board FPGAs
- Crate and system-level merging performed by single module design

The Common Merger Module



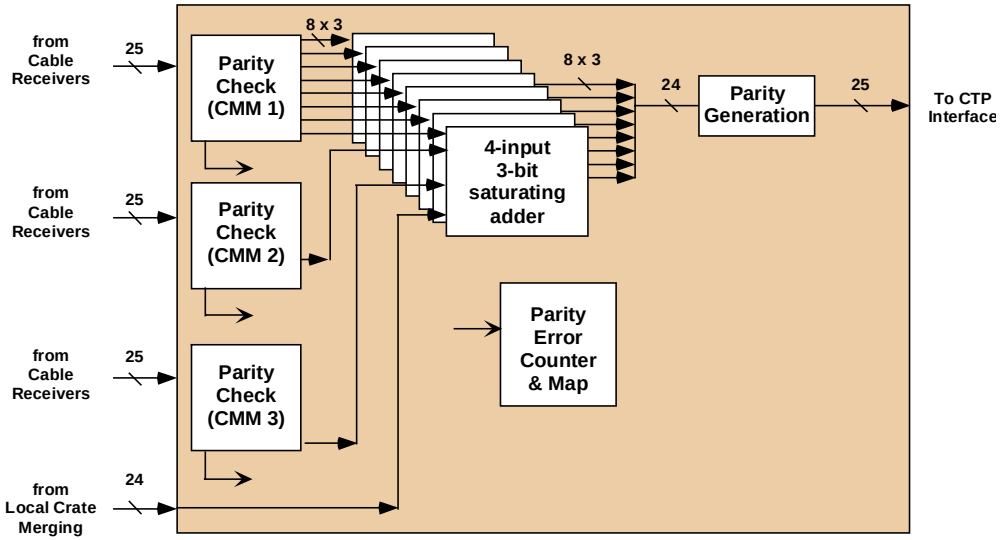
- Crate logic and system logic implemented in two XCV1000E FPGAs
- XCV1000E:
  - ~1.5 million gates
  - 96 × 4kbit block RAM
  - User IO = 660 pins (fine-pitch BGA)
  - Cost: ~ £690 (1600 CHF)
- Crate logic: large pin count required
- System logic: large number of LUTs required
- On-board Flash memories contain all FPGA configurations
- FPGAs configured to required type according to geographical address & crate no.

Firmware: CP Crate-level Merging



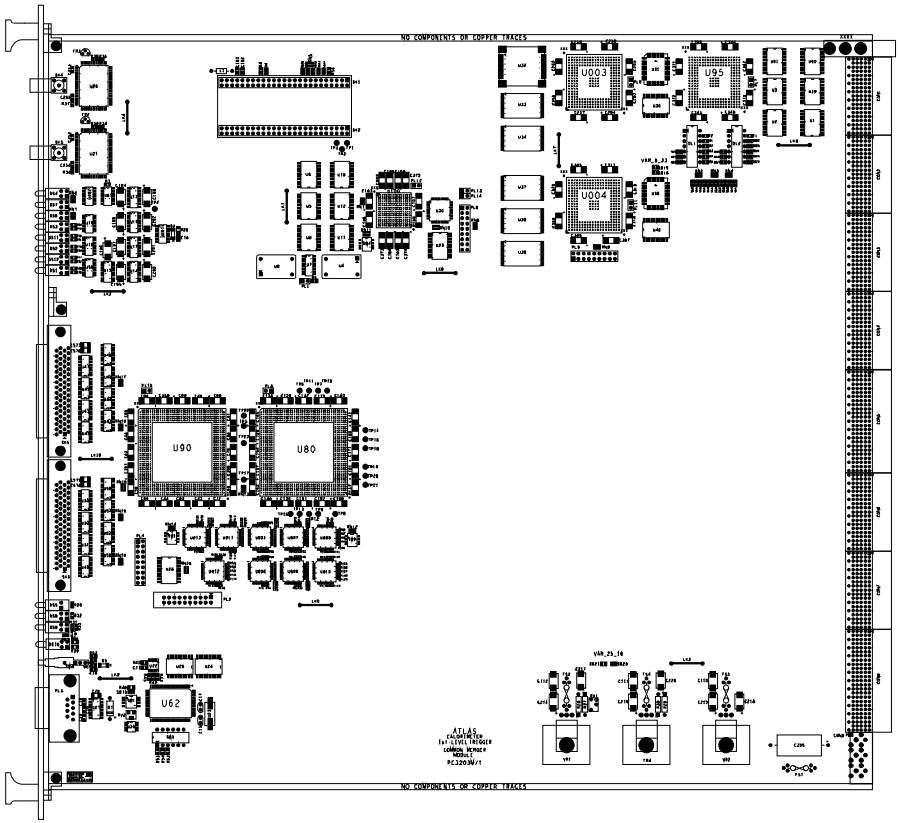
- Latency of real-time path
  = 3 BCs (optimised)
- FPGA also contains
  - readout buffers
  - readout controller
  - synchronisation logic
- Device utilisation (XCV1000E):
  - `Number of Slices:`
    `3,326 out of 12,288  27%`
  - `Number of Block RAMs:`
    `60 out of  96  62%`
  - `Number of bonded IOBs:`
    `457 out of  660  69%`

Firmware: CP System-level Merging



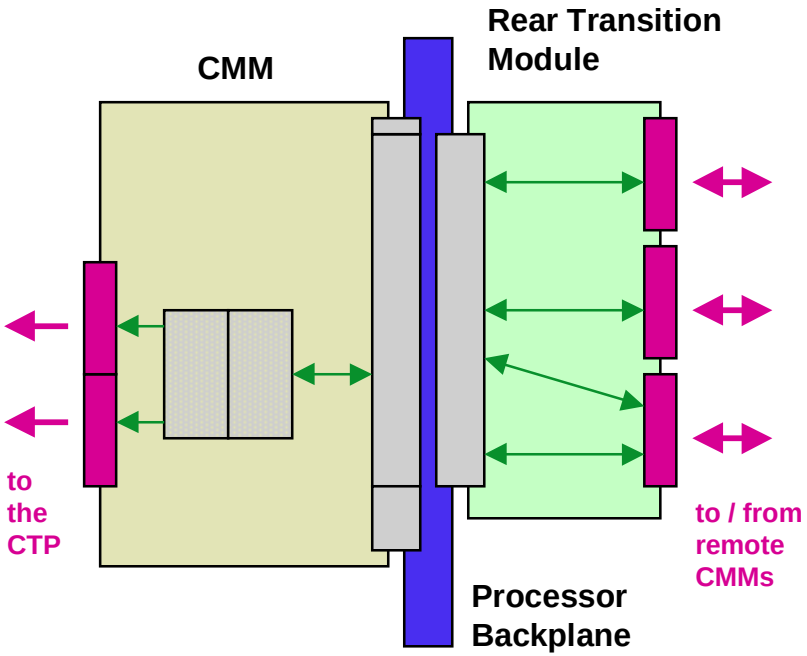
- Latency of real-time path = 3 BCs (not yet optimised)
- FPGA also contains
  - readout buffers
  - synchronisation logic
- Device utilisation (XCV1000E):
  - Number of Slices: 662 out of 12,288 5%
  - Number of bonded IOBs: 175 out of 660 26%
  - Number of Block RAMs: 16 out of 96 16%

CMM Layout



- 12 Layer board
- High density of tracks into 2 FPGAs
- Some uncertainty regarding required position of backplane connectors; now resolved

Rear Transition Module & Cables



Rear Transition Module (RTM):

- Passive module
- Mounts ≤ 3 cables carrying data between Crate & System CMMs
- Passes signals through backplane to CMM
- Provides cable ground

Connectors / Cables:

- For test purposes, use connectors of same type on
  - CMM front panel
  - Rear Transition Module
  - DSS LVDS source/sink card
- Format chosen = SCSI-3, 68-way:
  - Off-the-shelf
  - Known specification
  - Patch panel to CTP(D) required

Status & Schedule

CMM Firmware

- e/γ & τ/hadron Crate-level CMM ✓
- e/γ & τ/hadron System-level CMM ✓
- Jet Crate-level CMM ×
- Jet System-level CMM ×
- Energy Crate-level CMM ×
- Energy System-level CMM ×

CMM Hardware

- Schematic capture finished June 2001
- Board to manufacture mid-November 2001
- Stand-alone tests December 2001
- System tests January 2001

Other Hardware

- Rear Transition Module
  - Schematic capture in progress
  - Queued for drawing office
- DSS LVDS source/sink card
  - Schematic capture completed
  - To Drawing Office immediately after CMM.

Conclusion

CMM on schedule to be ready for Level-1 slice tests next year.