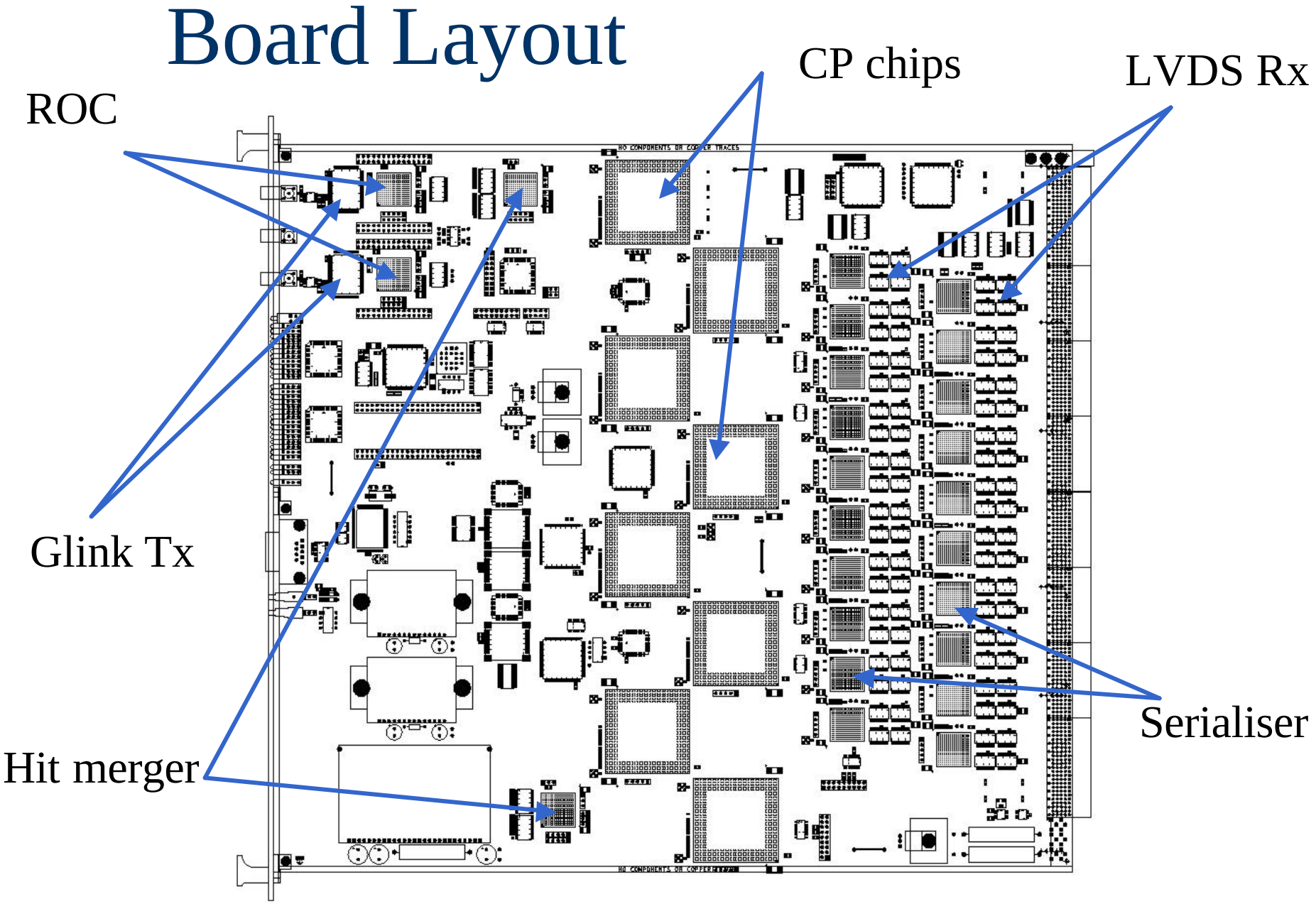
Cluster Processor Module

Status and future

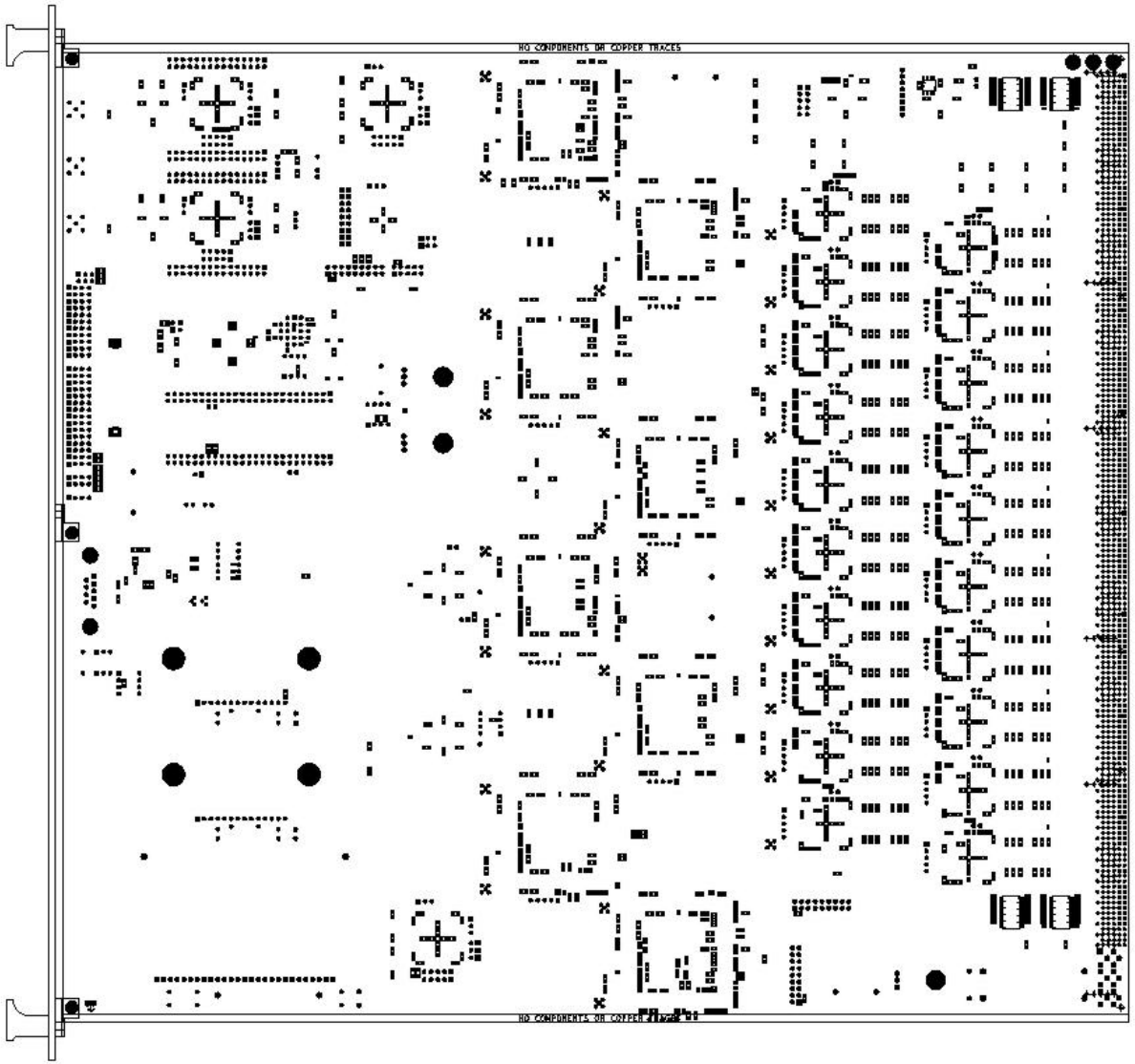
Schematic Status

- August 01: schematic finished, send to RAL drawing office
- September 01: Netlist checked
- November 01: 25 % components placed and routed:
  - 4 IC’s only on back side (buffer)
  - 1500 R’s and C’s
  - 24000 Pins
  - 16 layers
  - 4000 signal nets
  - 32 BGA (8 Fine Pitch)

Board Layout



Board Layout (BackSide)



Debugging

- Silk screen with pin number around connector
- Connector: re-route signals
- Testpoints:
  - Clock
  - ROC: 8 pins
  - SRL:4 pins in common with CP, 4 spares as bus
  - CPchip: 4 pins in common with SRL, 4 spares, 4 spares as bus
  - hit mergers: 2(1 + 8) bit threshold to LED display
  - 20 bits Glink input
  - VME controller: 4 pins
  - More…

Testing

- Concurrent CPU board successfully installed @ bham (thanks Bruce):
  - Same one as RAL
- HDMC V0.2, RH7.0
- First access to our local crate done: VMEBusCct
- Play with TTCvi module

Next things to do…

- H/W:
  - Complete/update F/W: add registers with F/W version, …
  - Start putting F/W code on the web: http://hepunx.rl.ac.uk/cgi-bin/csweb.cgi/firmware
  - Update documentation
- S/W:
  - Write CPM parts
  - Write CPM testing code/ Module services