Implementation of the Jet Algorithm

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Anders Ferm

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We are rewriting the Jet algorithm from scratch

- Full-size algorithm (11x7)
- Produce portable VHDL code
- Take advantage of modern design tools (FPGA Advantage)
- Chance to examine and reevaluate algorithm elements and organisation

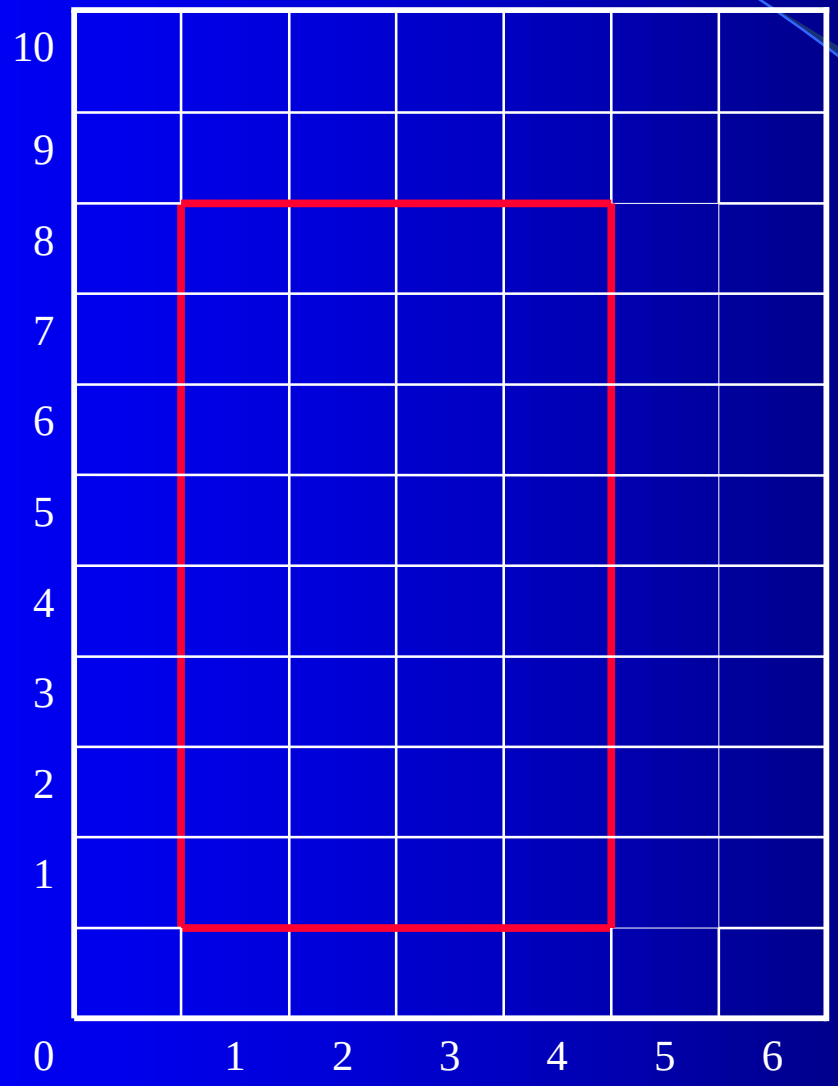
Strategy: Compact Design

- Design logic blocks that use as few resources as possible
  - 5-bit serial vs. 10-bit parallel
- Eliminate duplicated operations
  - Adder trees
  - Nearest neighbor comparison

Some examples from the algorithm

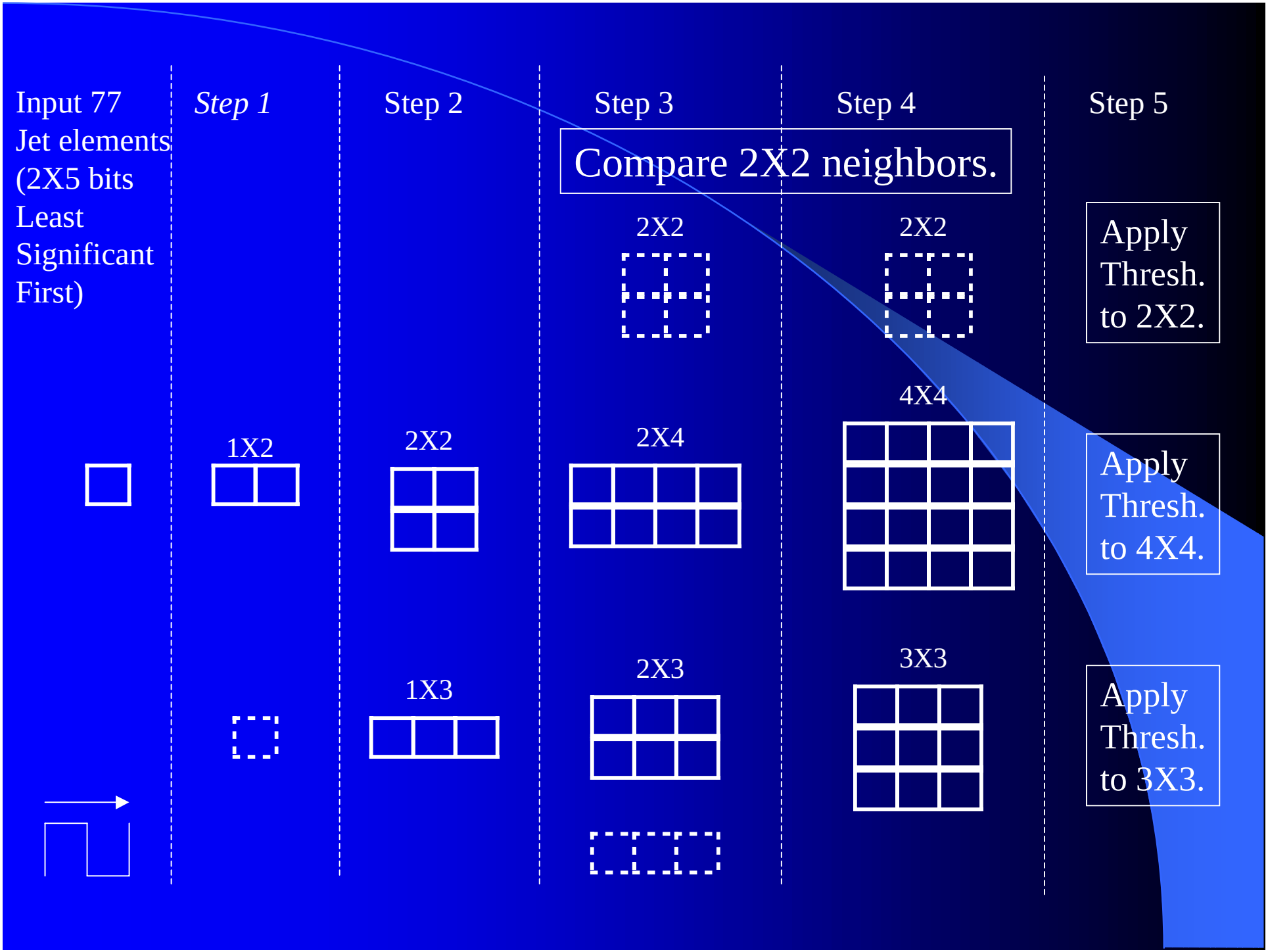
- The adder trees
- Local maximum identification

The Jet adder trees



77 Jet elements

32 Core elements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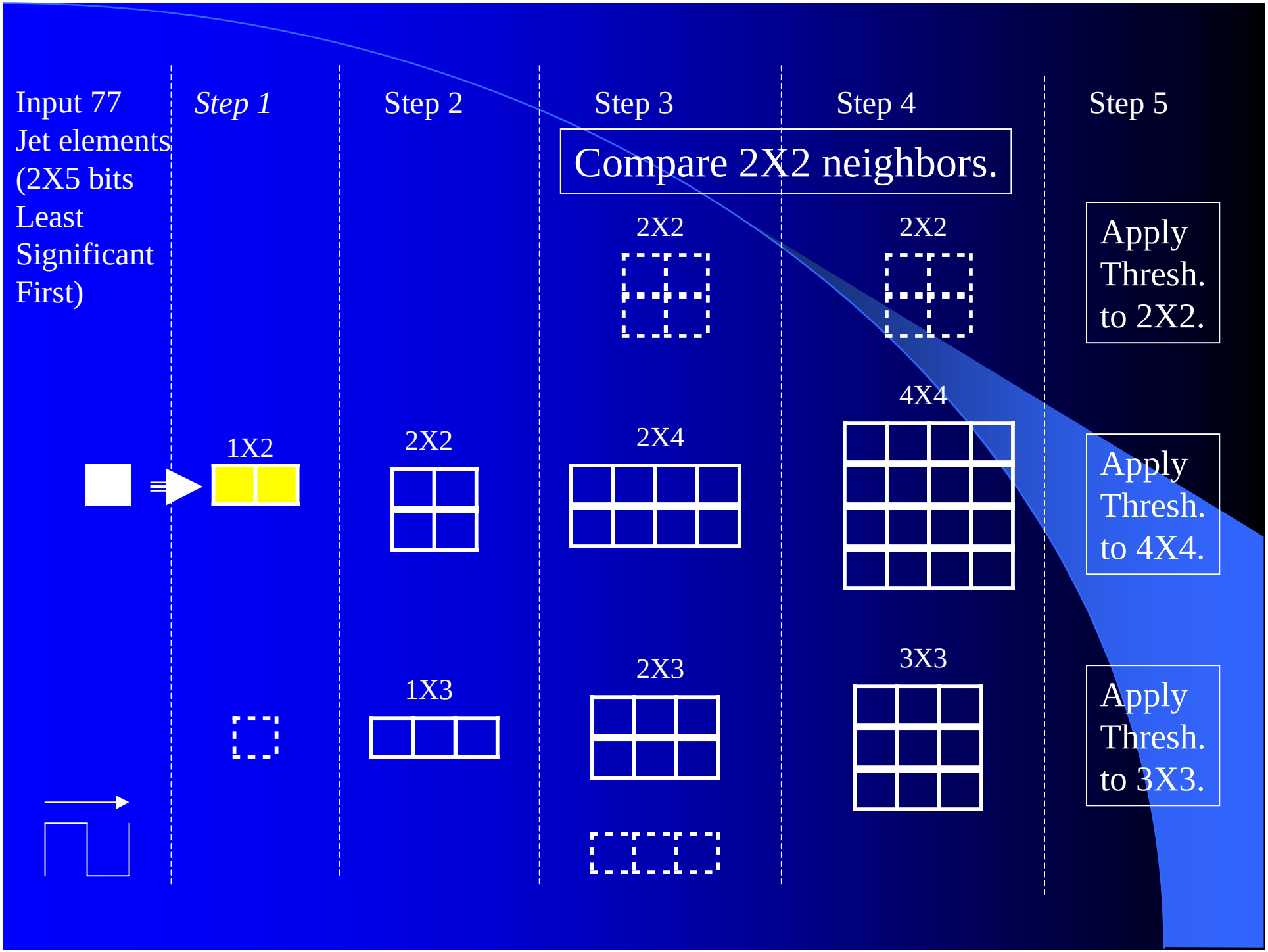
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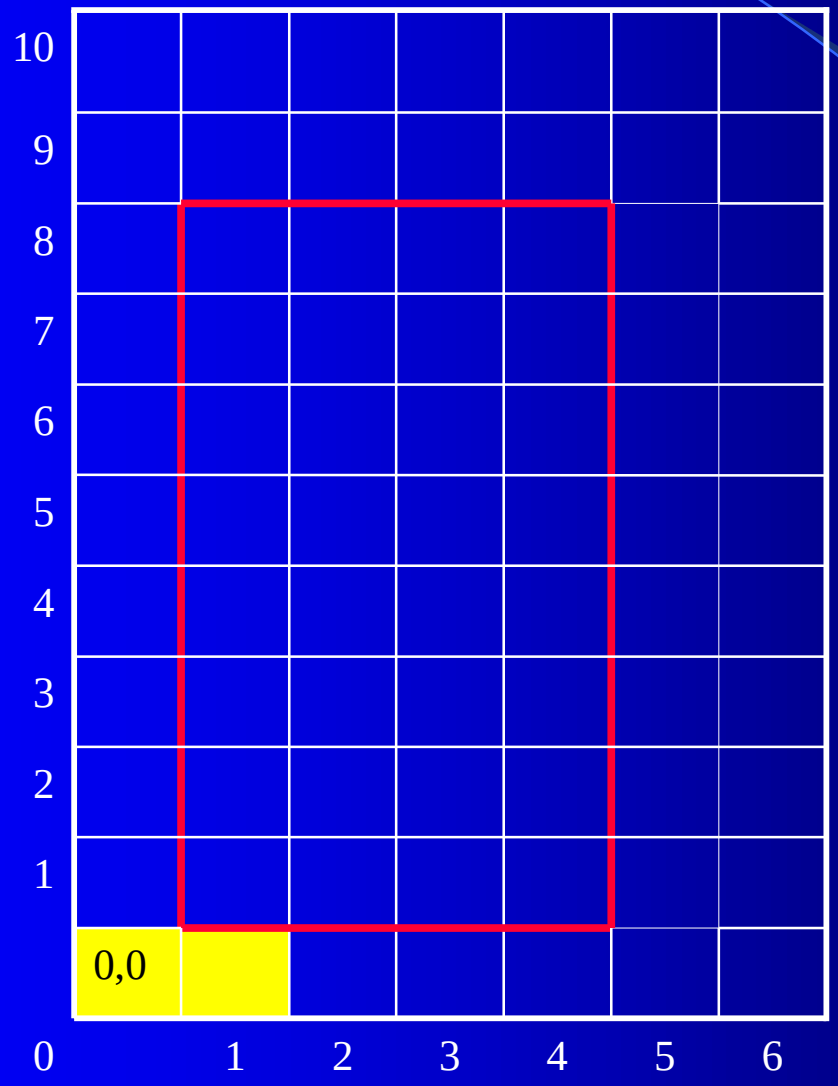
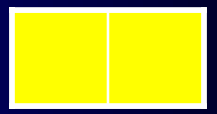
1x2 Jet element Sum (Step 1)



Total 1 summation



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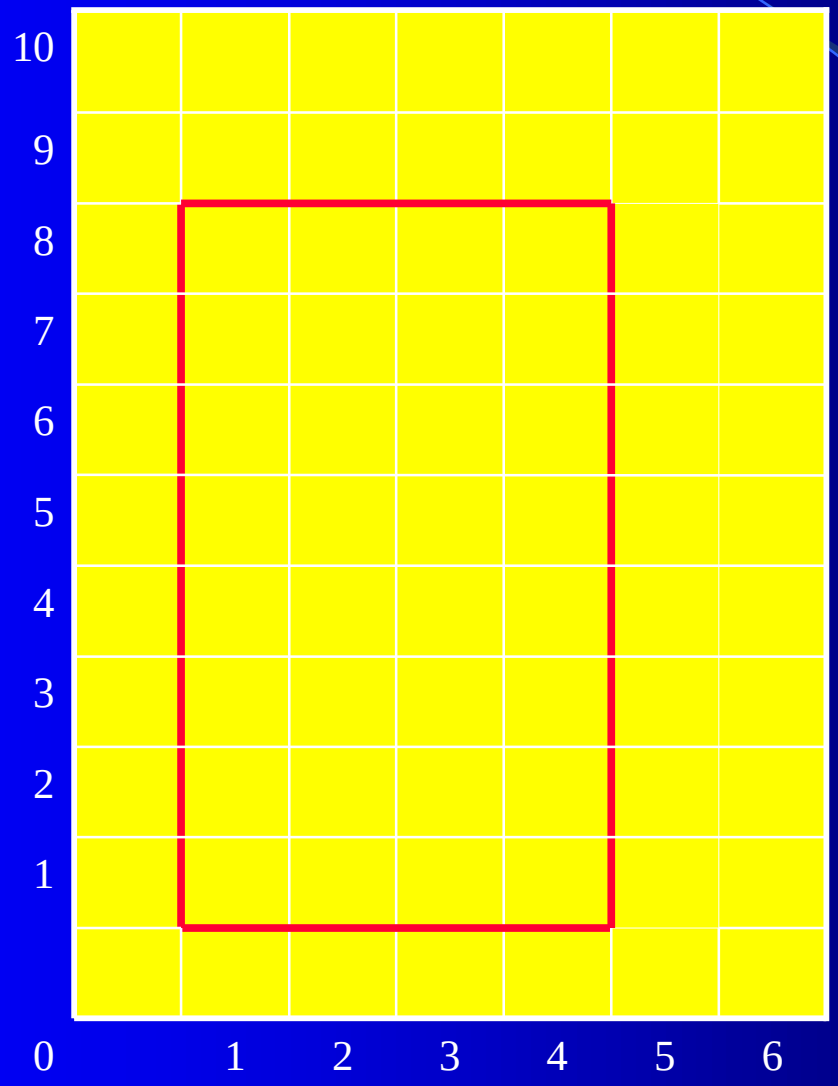
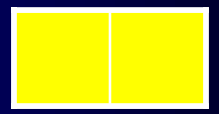
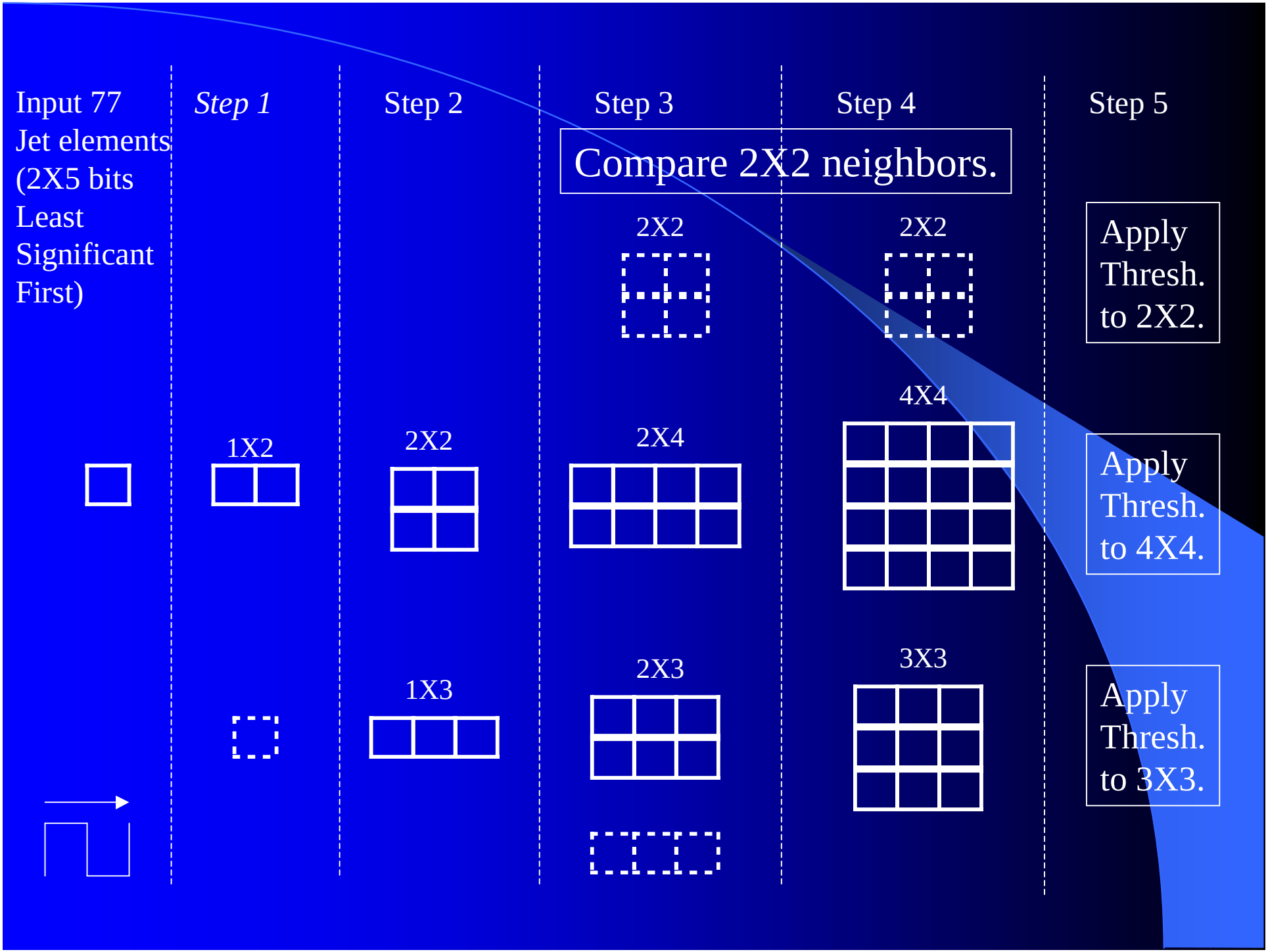


Total 11x6 summations

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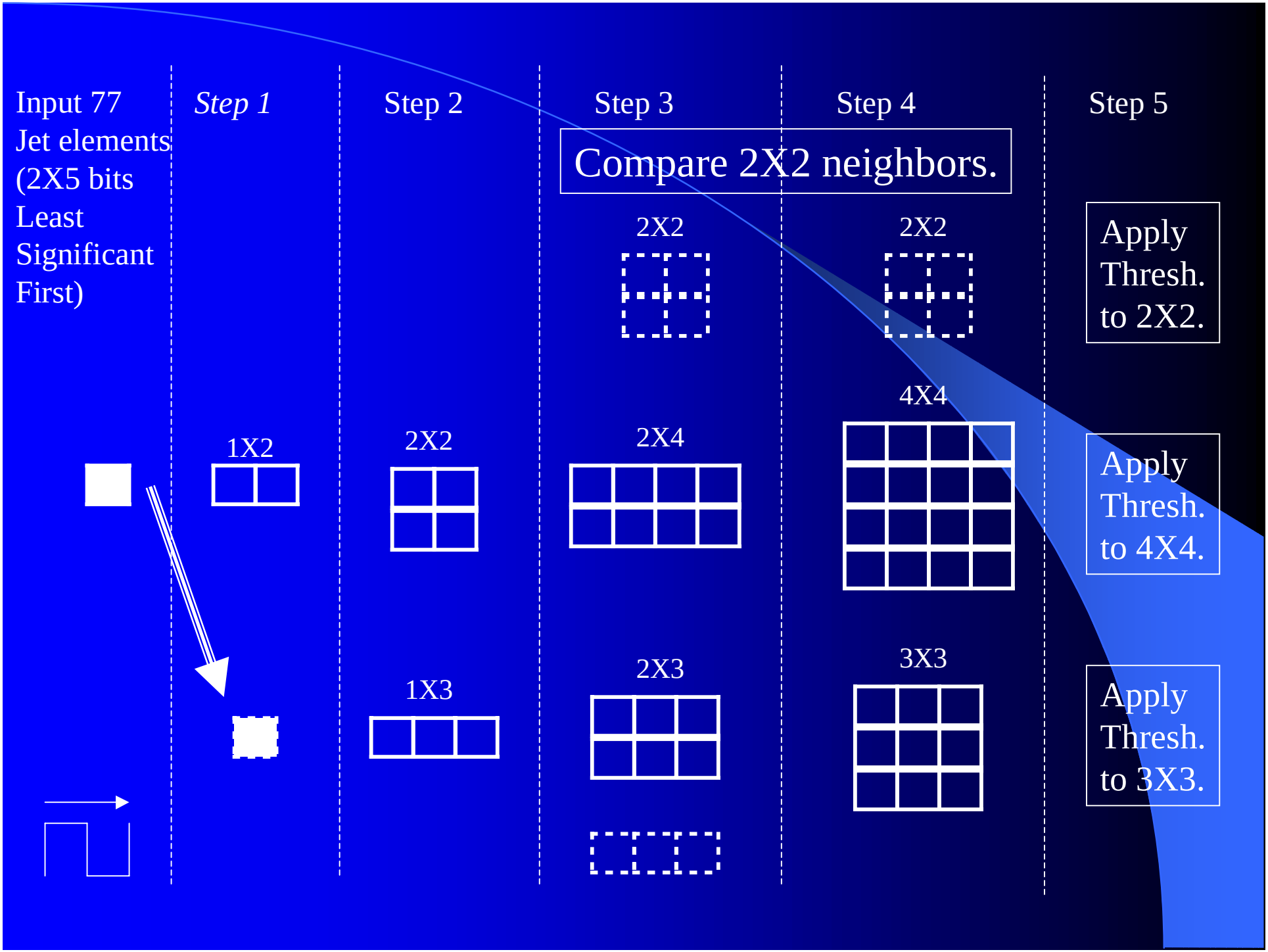
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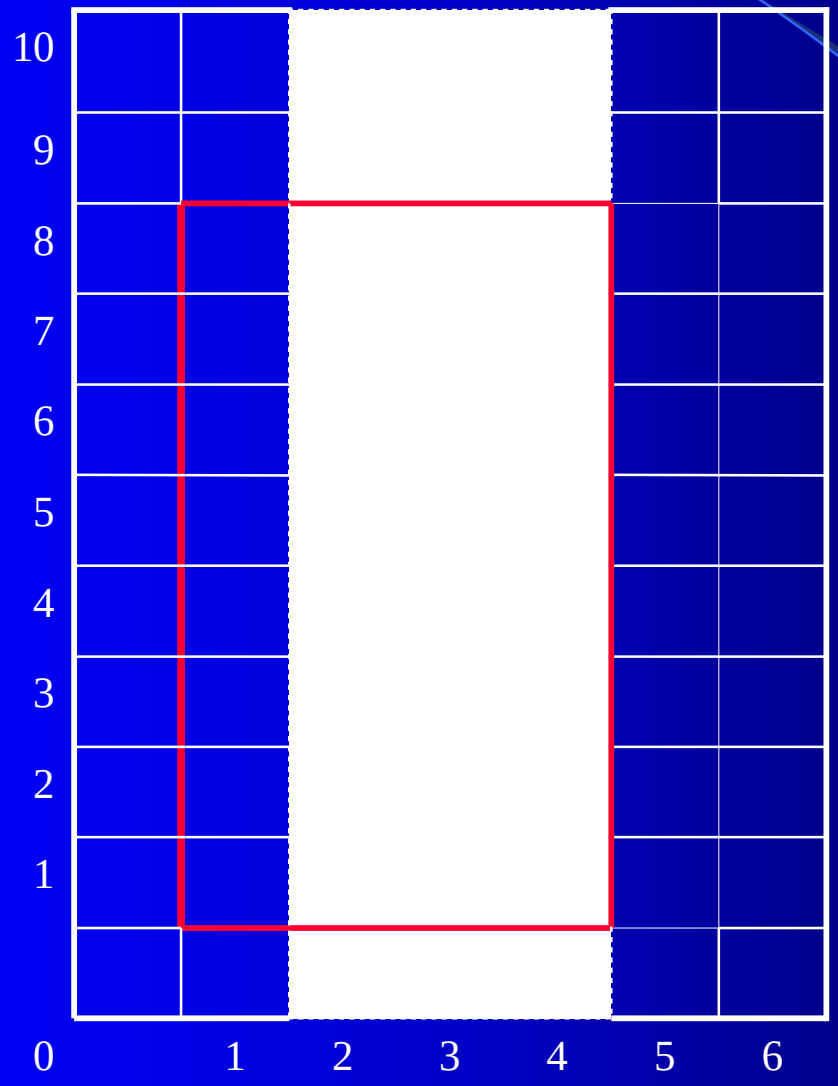
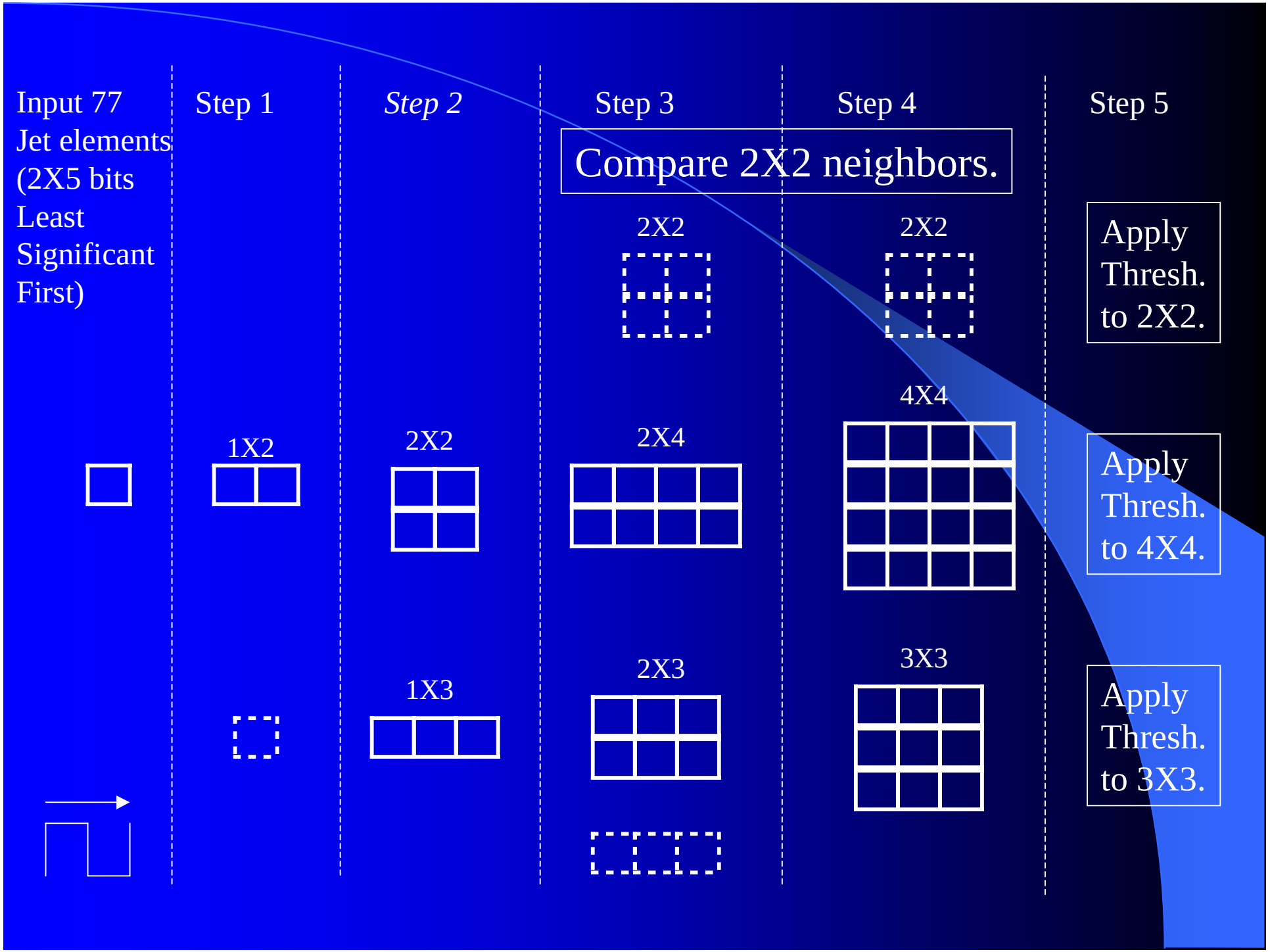
1x1 Jet element Save (Step 1)



Save 30 Jet elements
for the 1X3 summations.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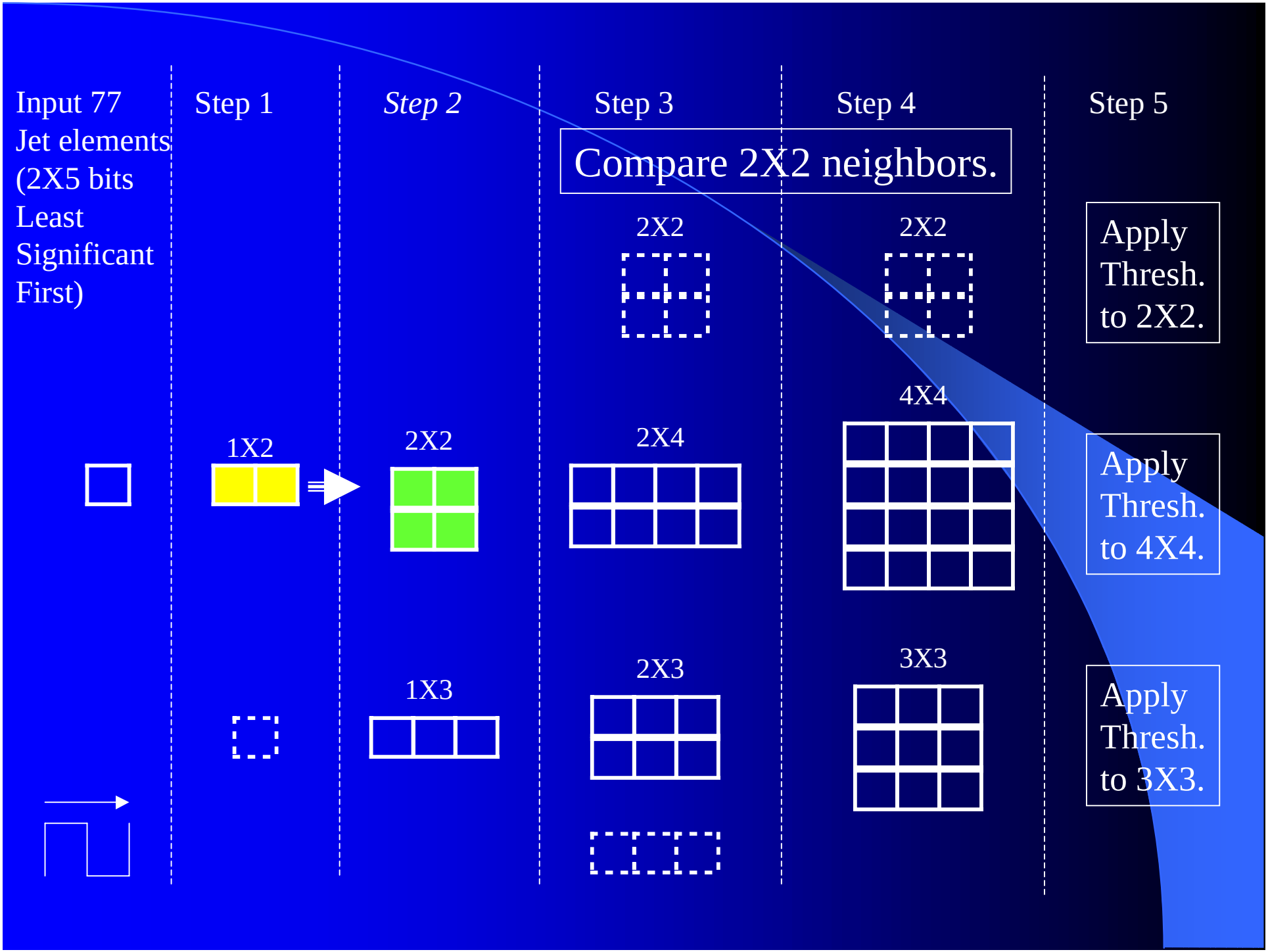
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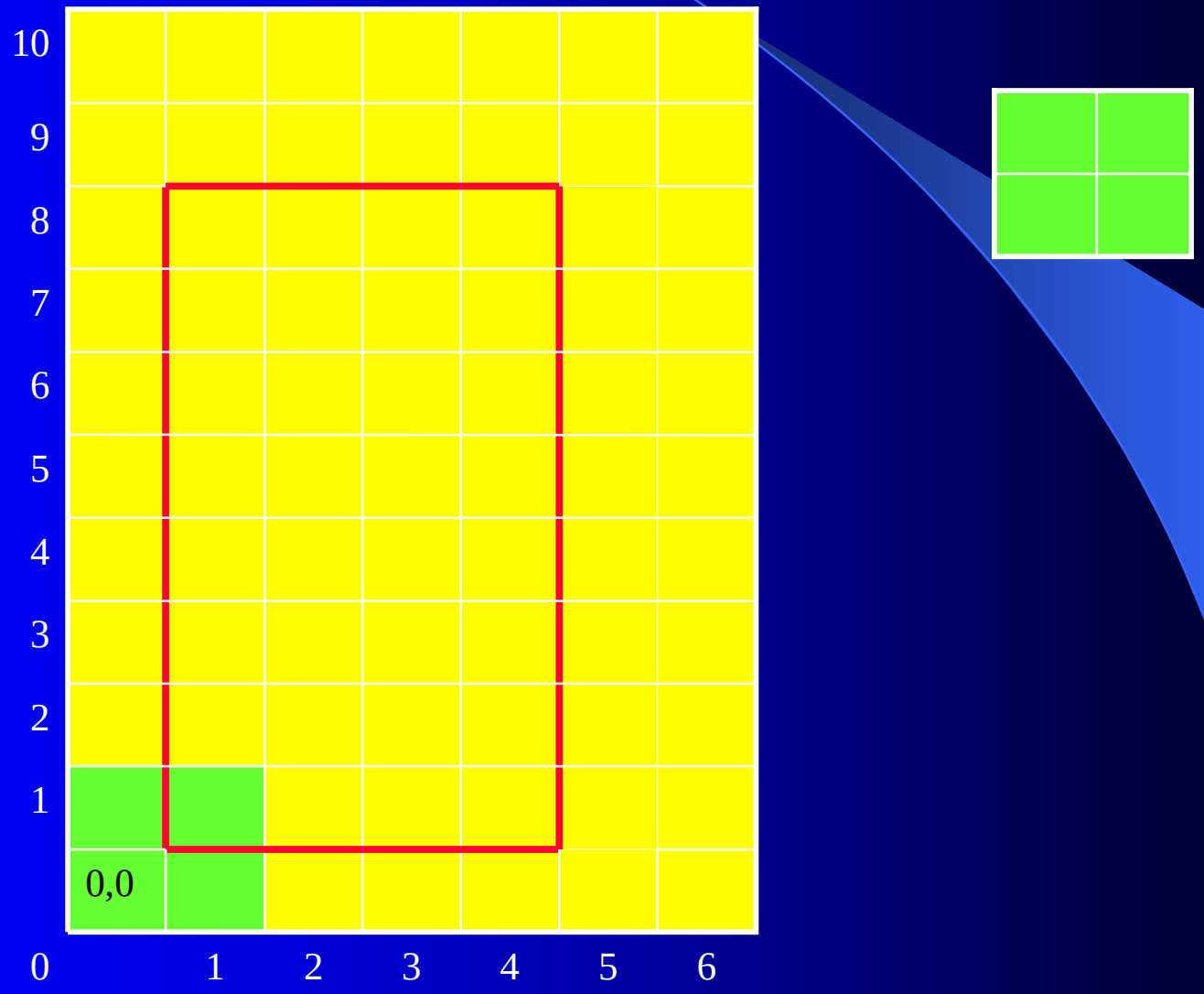
2x2 Jet element Sum (Step 2)



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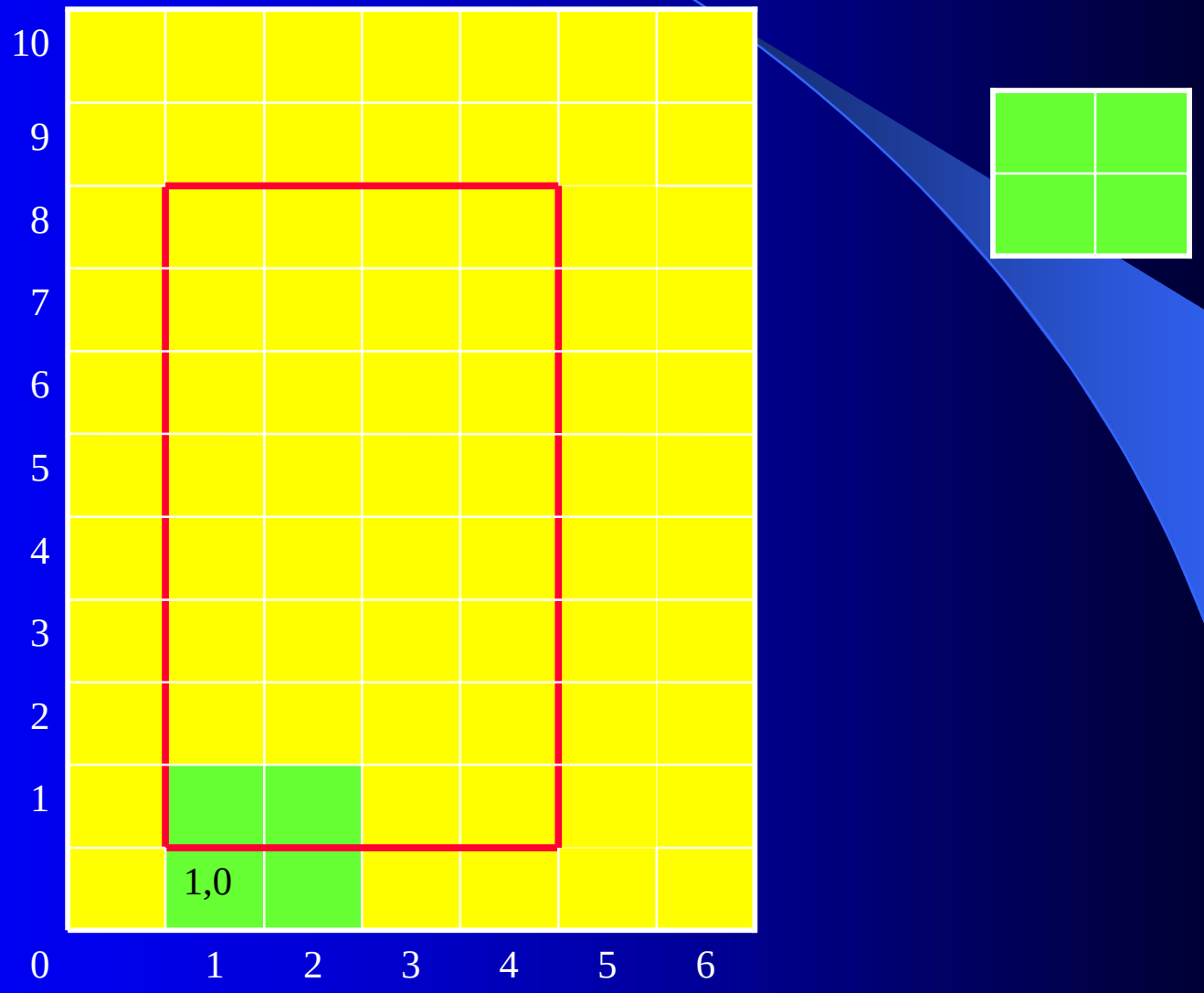

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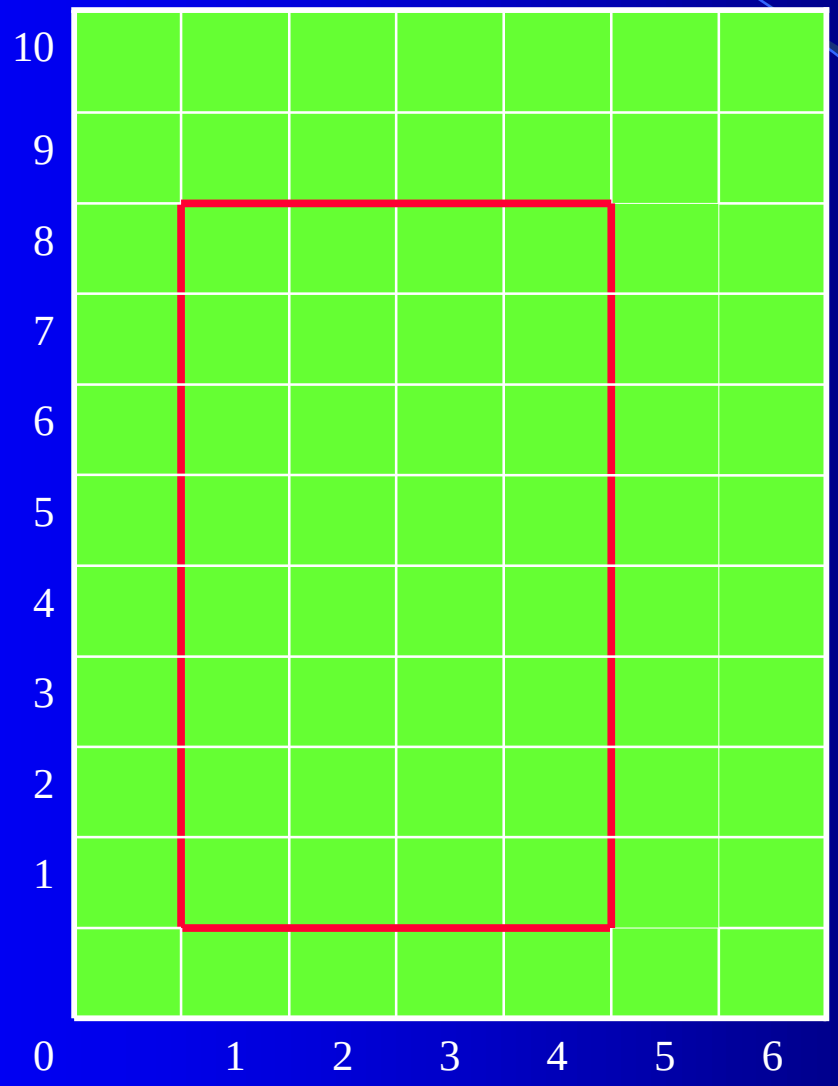
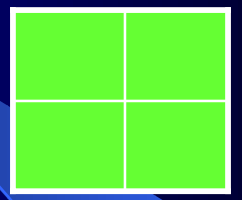
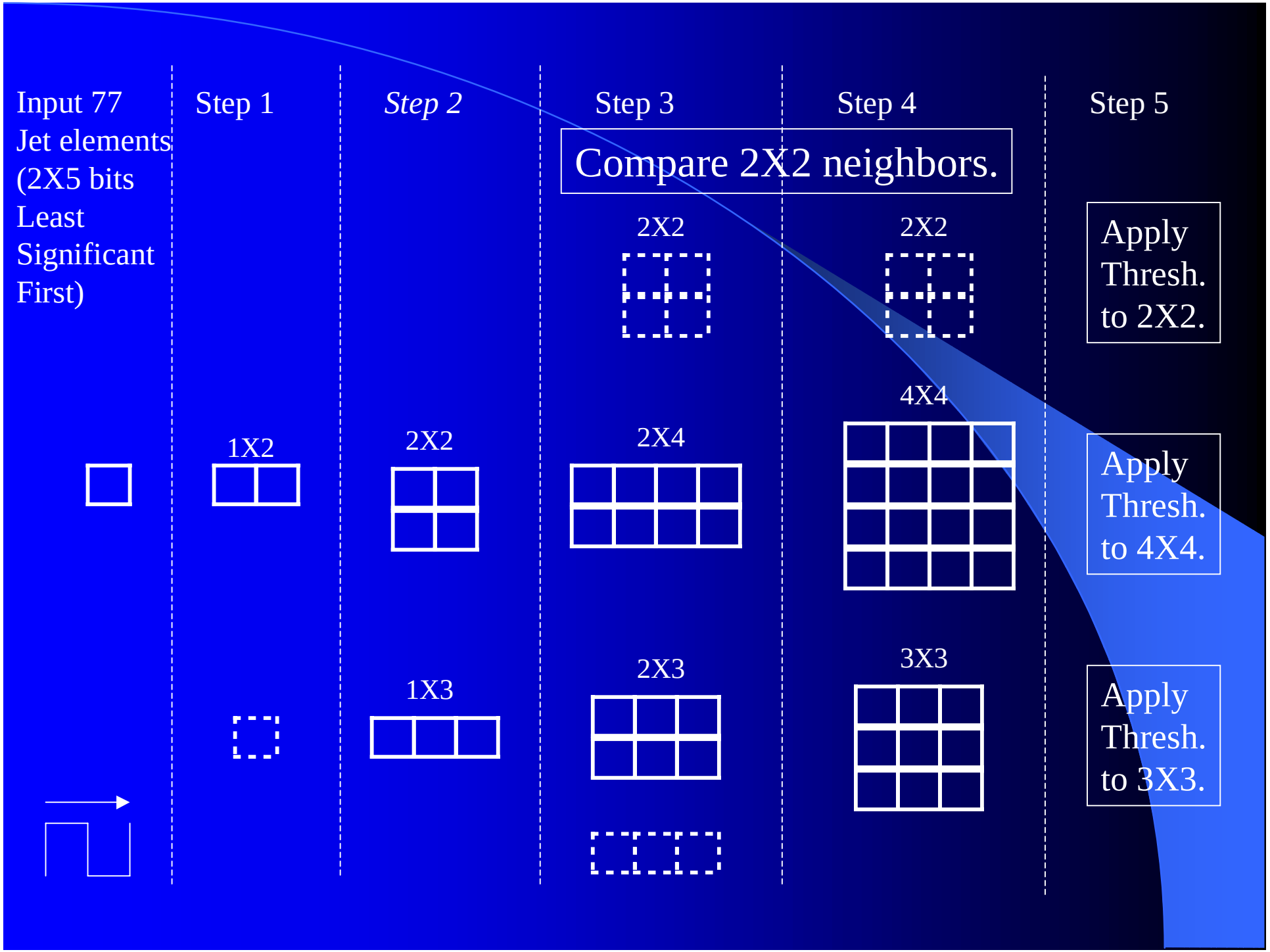


Total 10x6 summations

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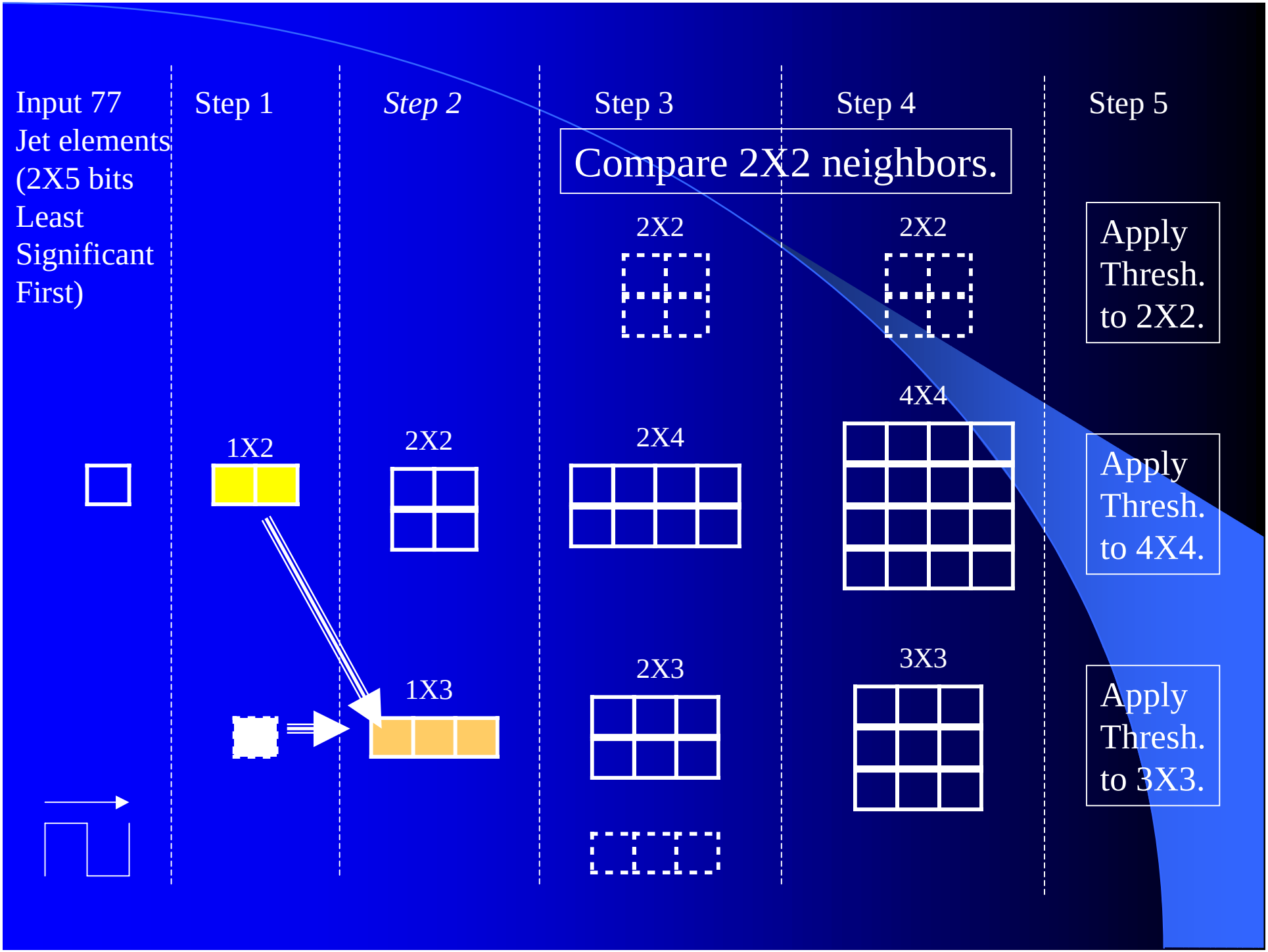
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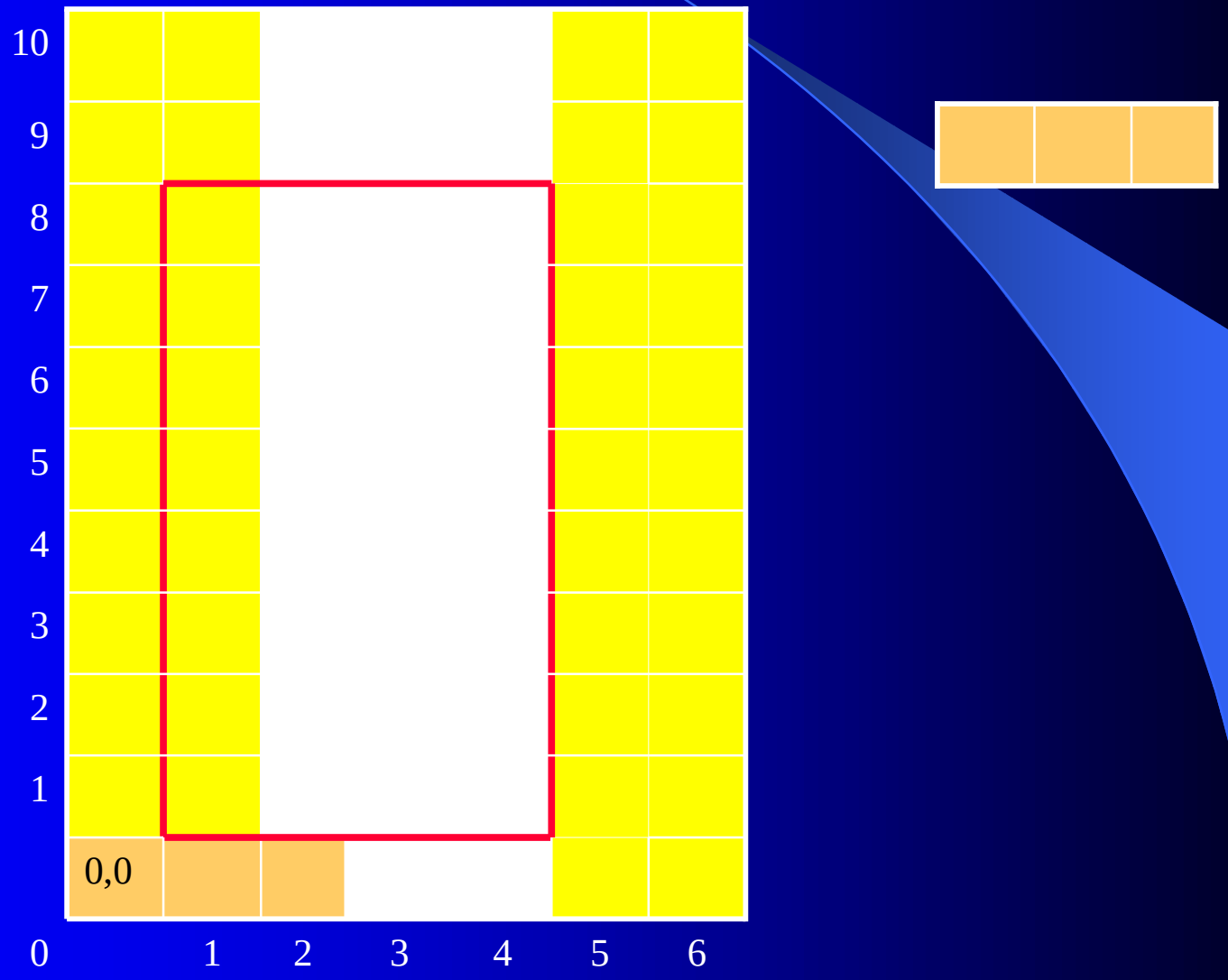
1x3 Jet element Sum (Step 2)



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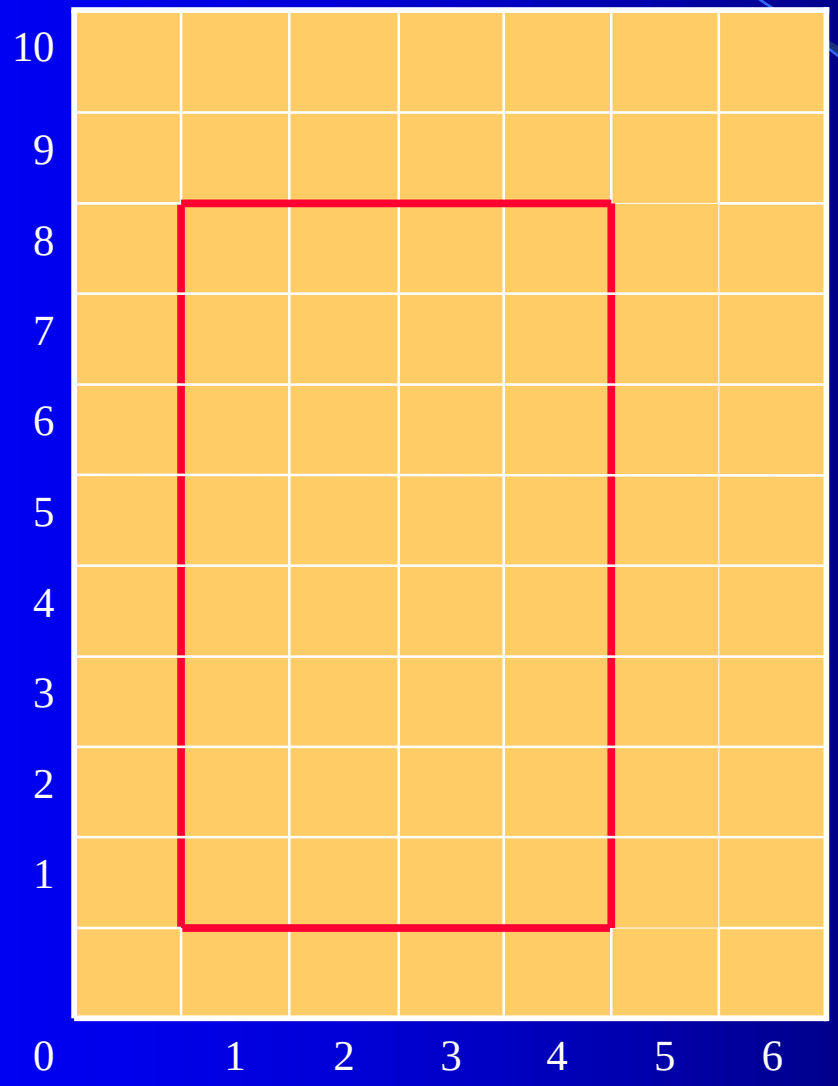

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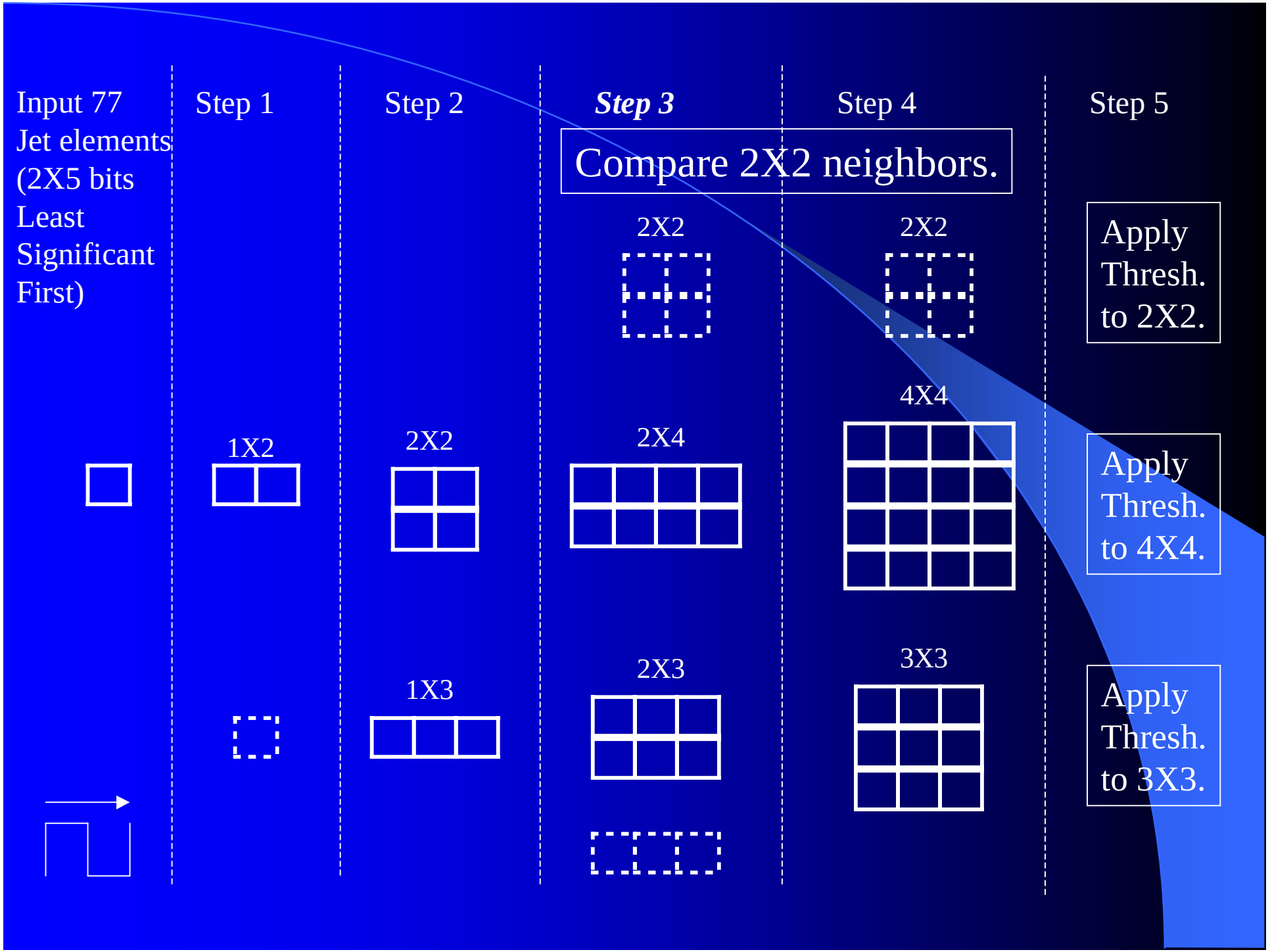
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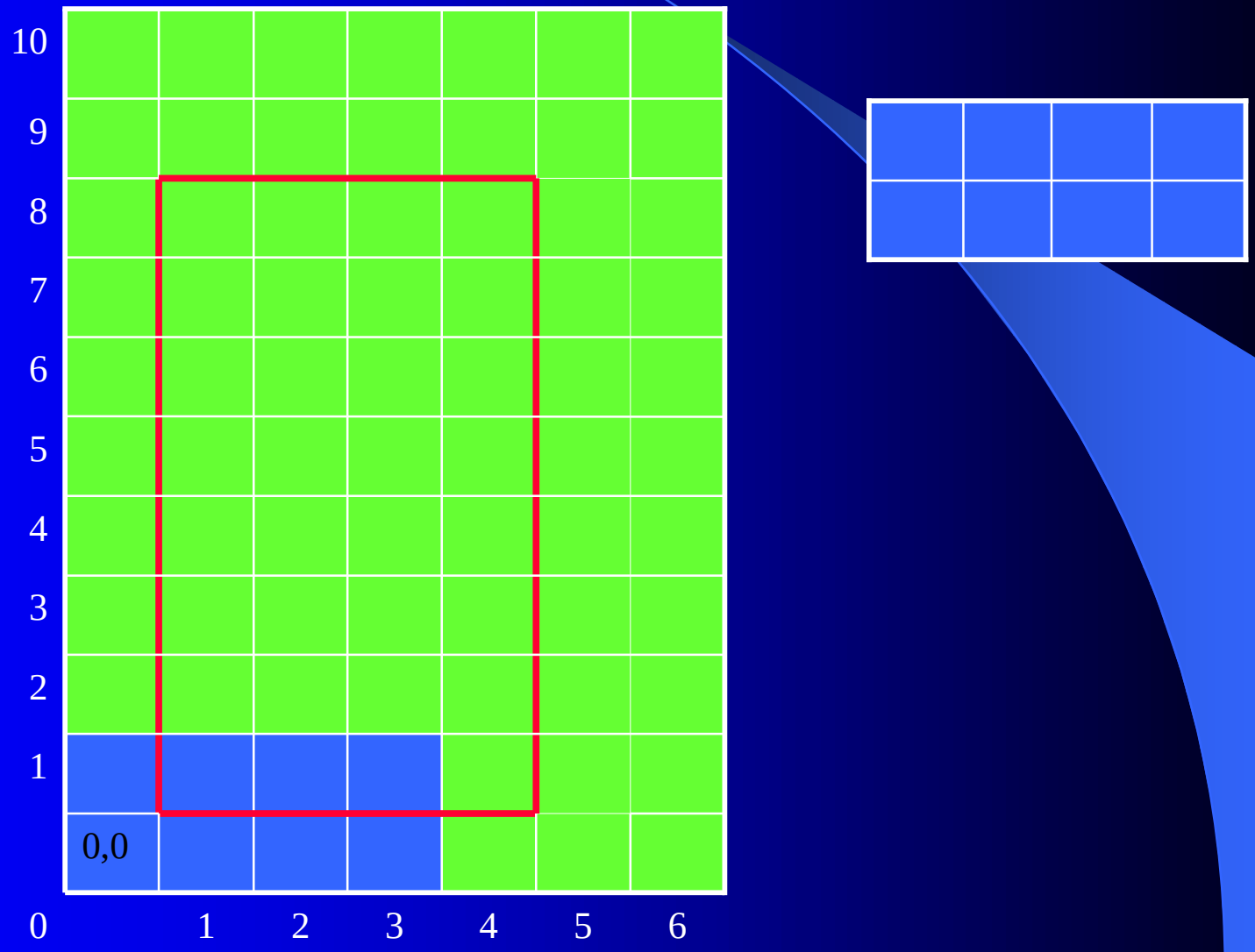
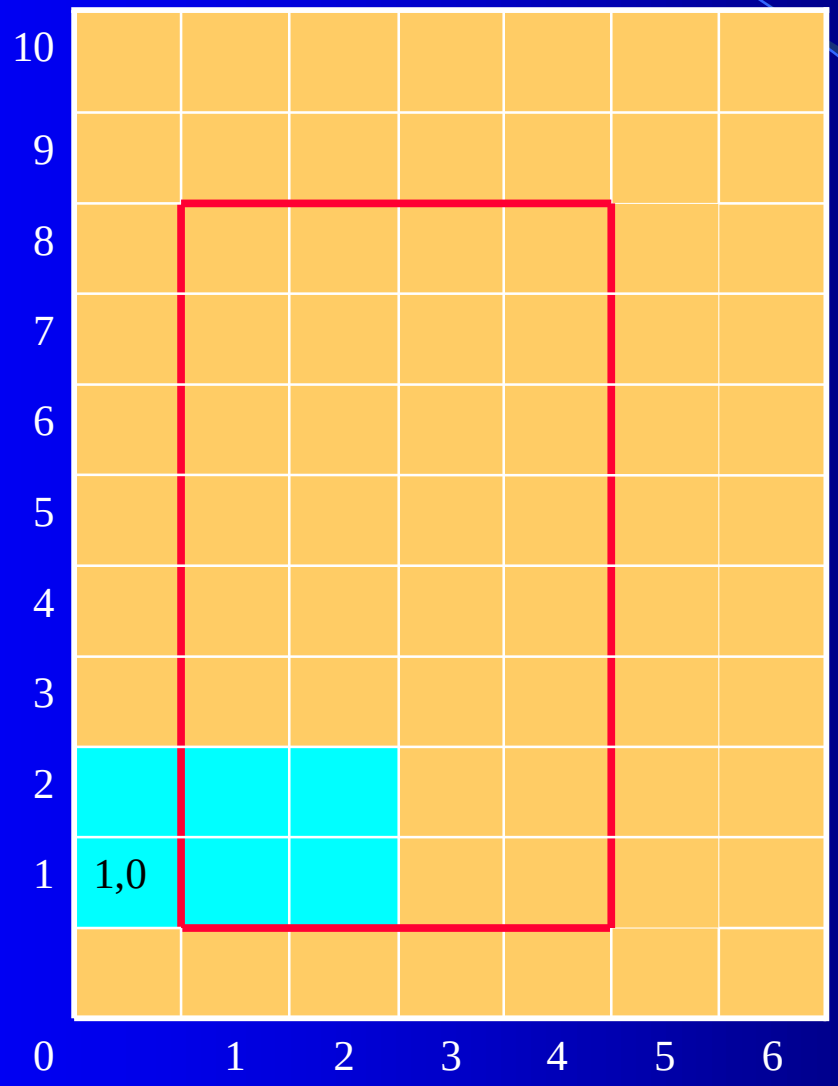
2x4 Jet element Sum (Step 3)



2x3 Jet element Sum (Step 3)



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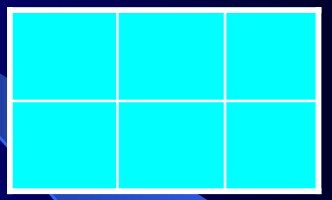

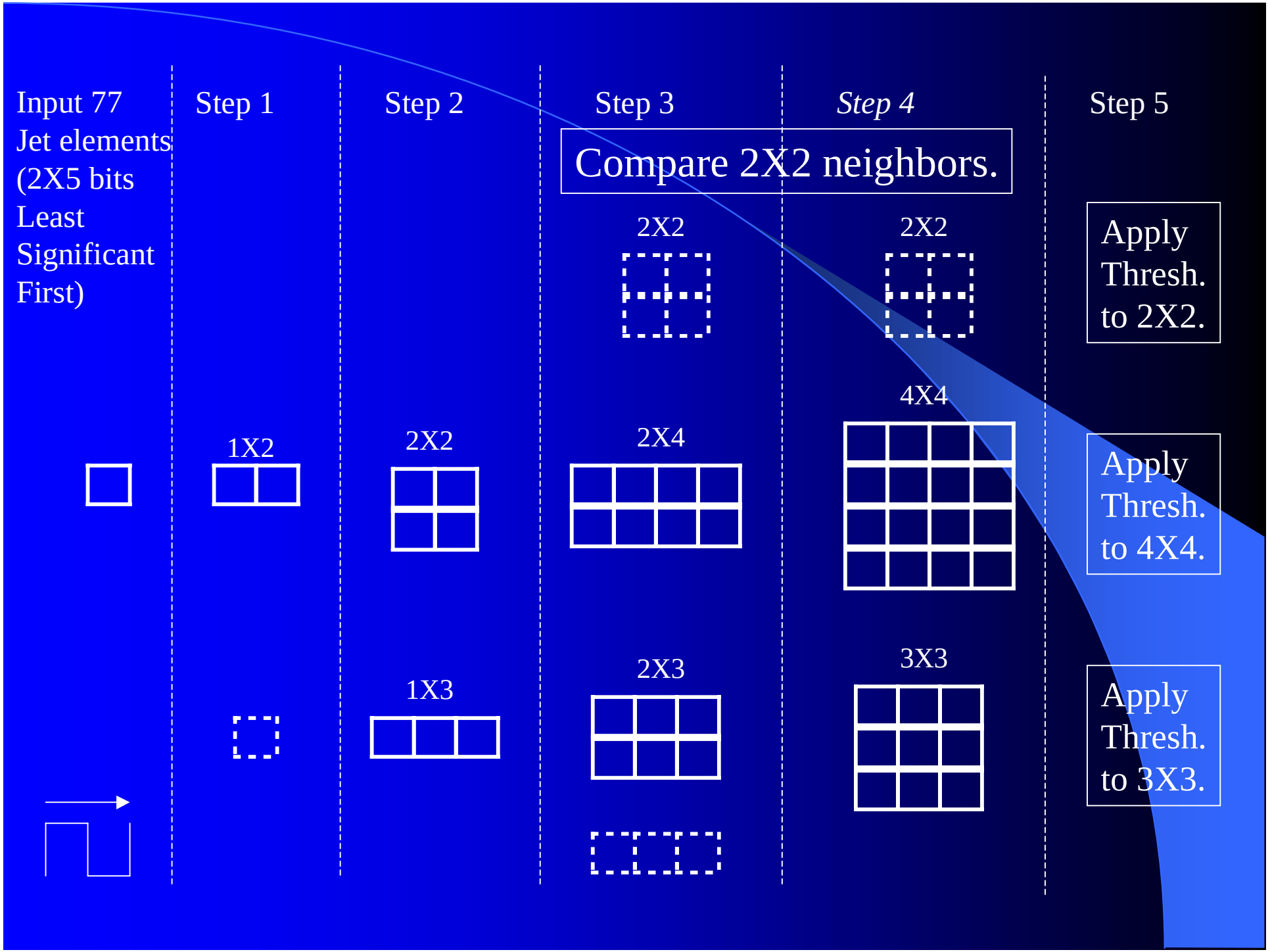
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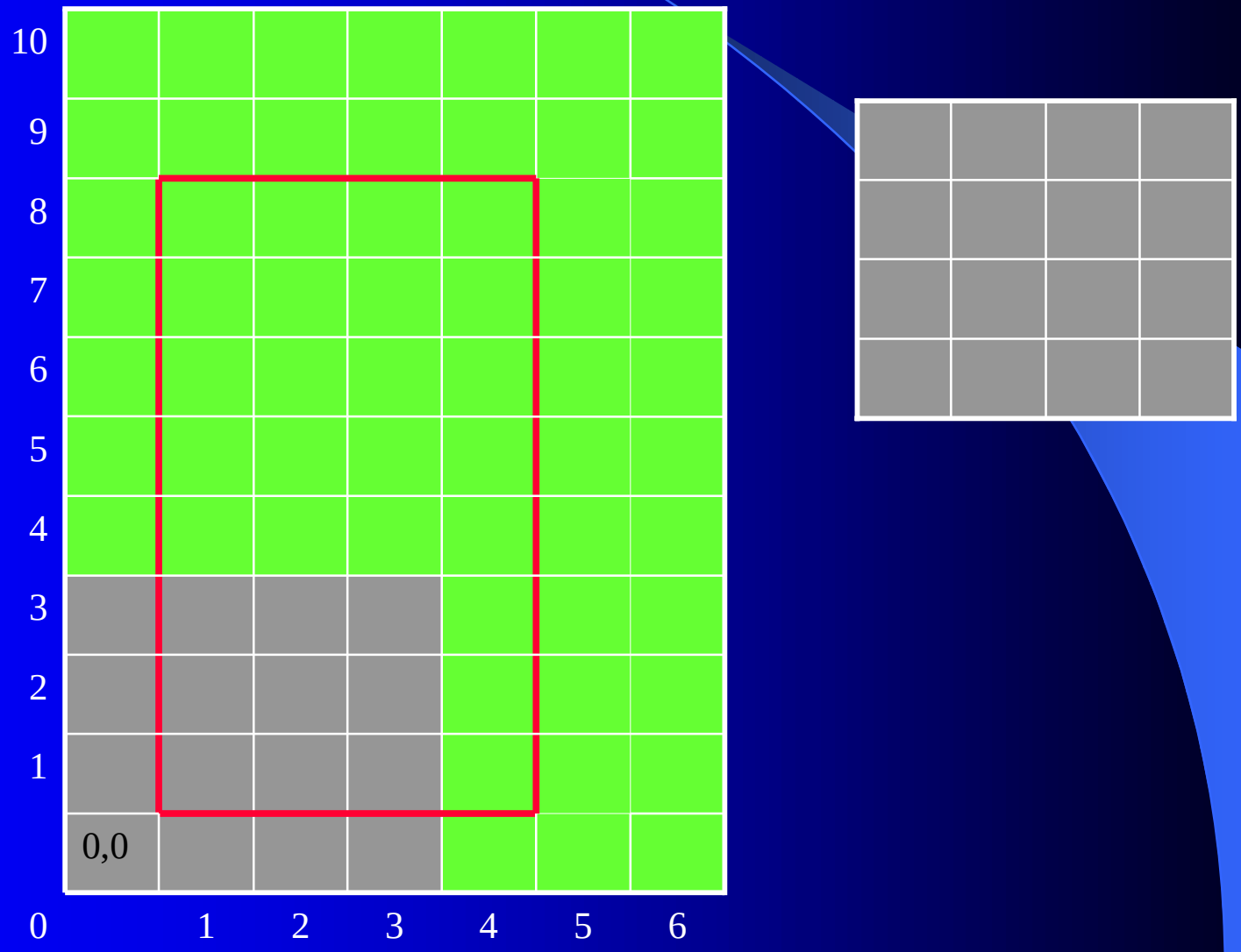
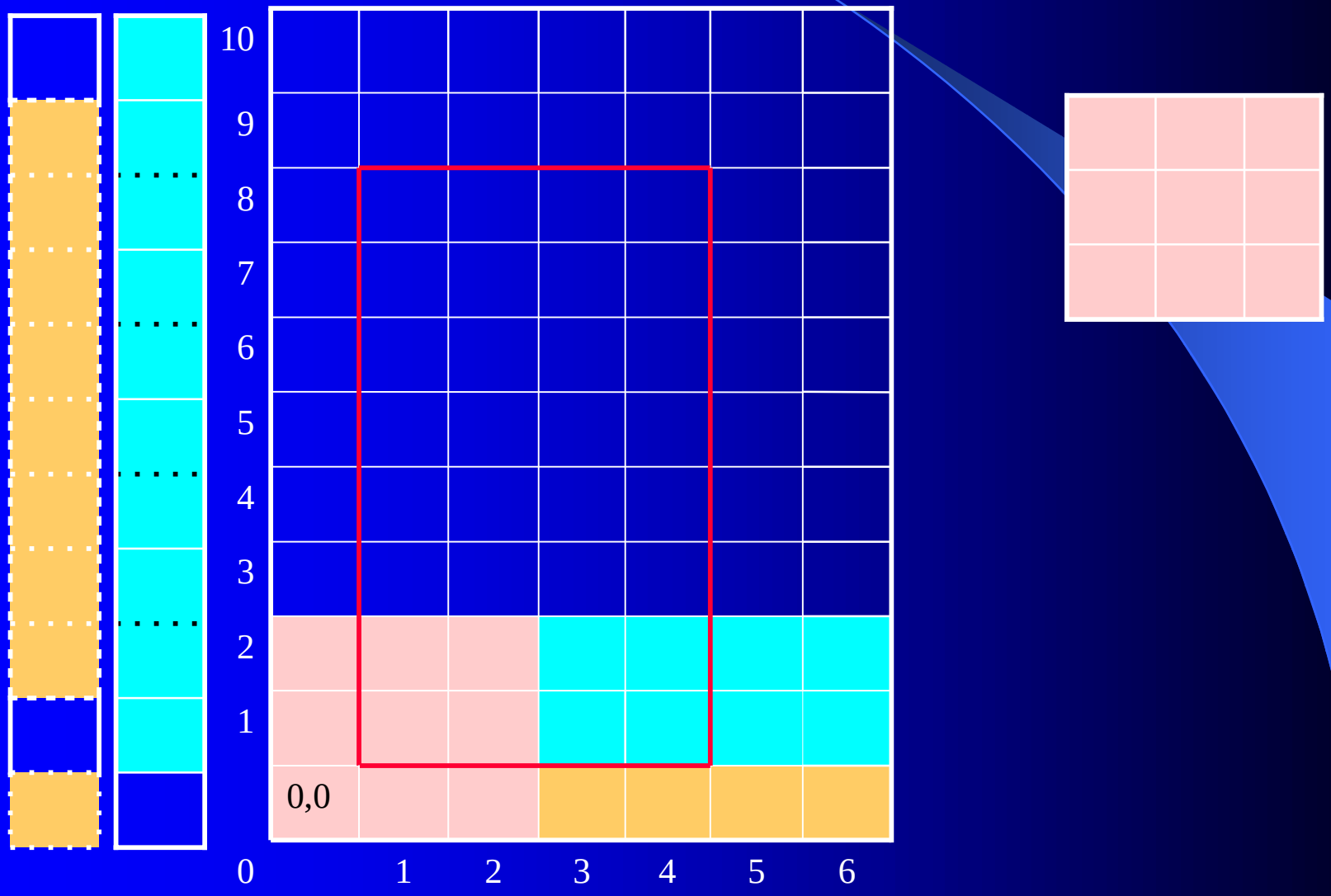
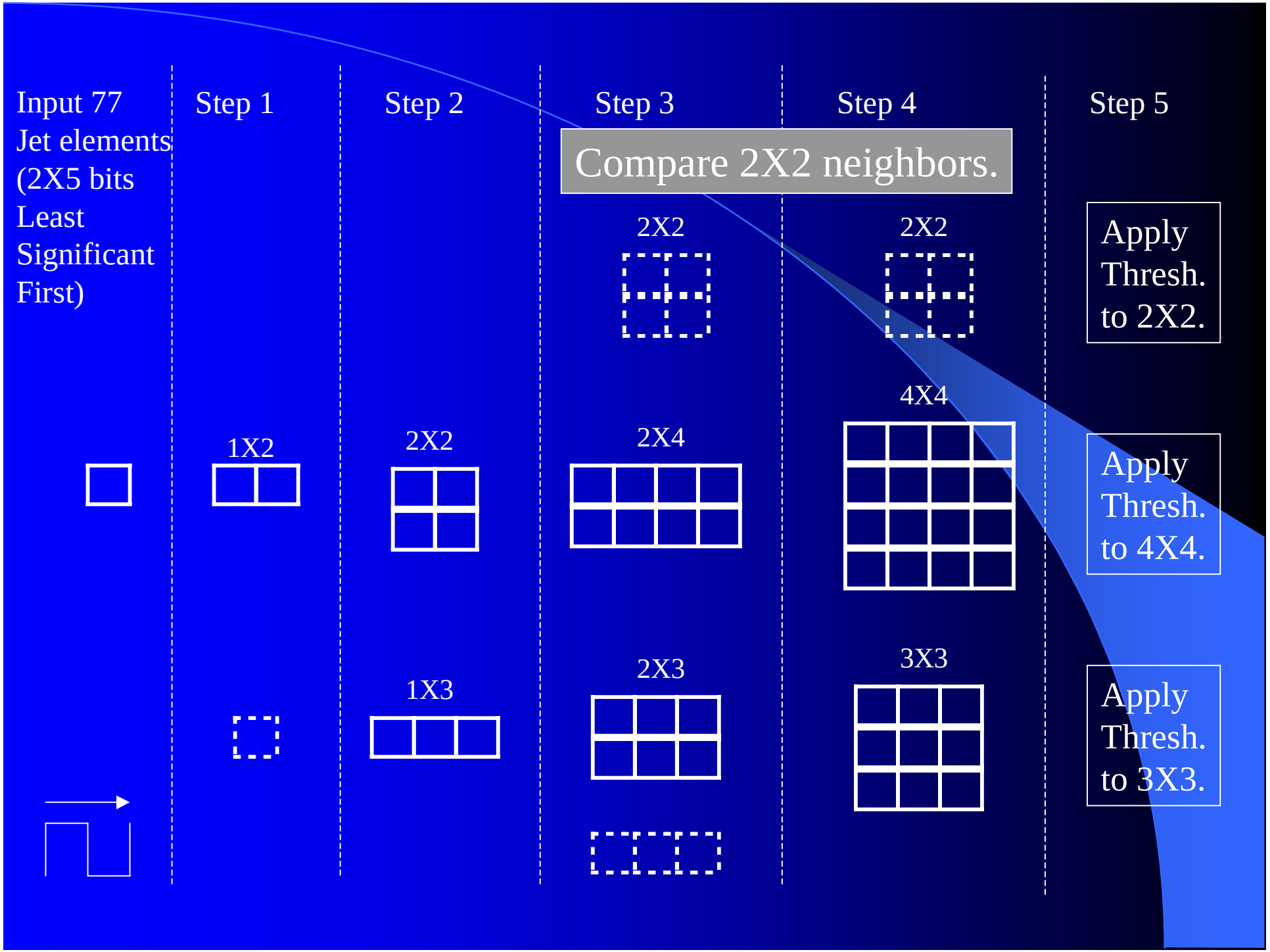
4x4 Jet element Sum (Step 4)



3x3 Jet element Sum (Step 4)

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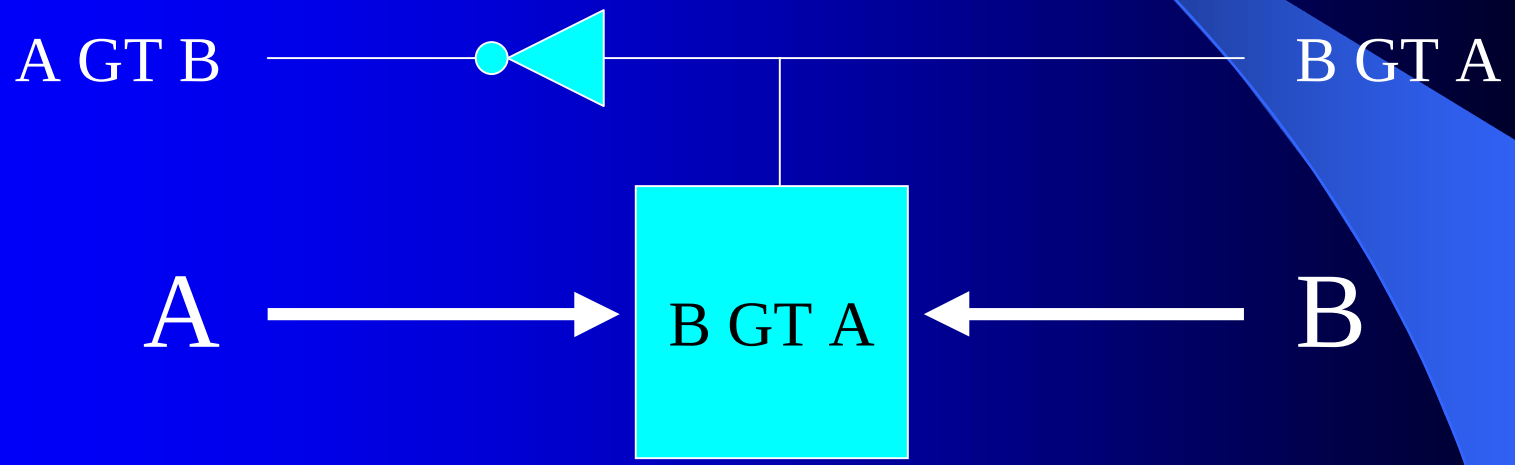
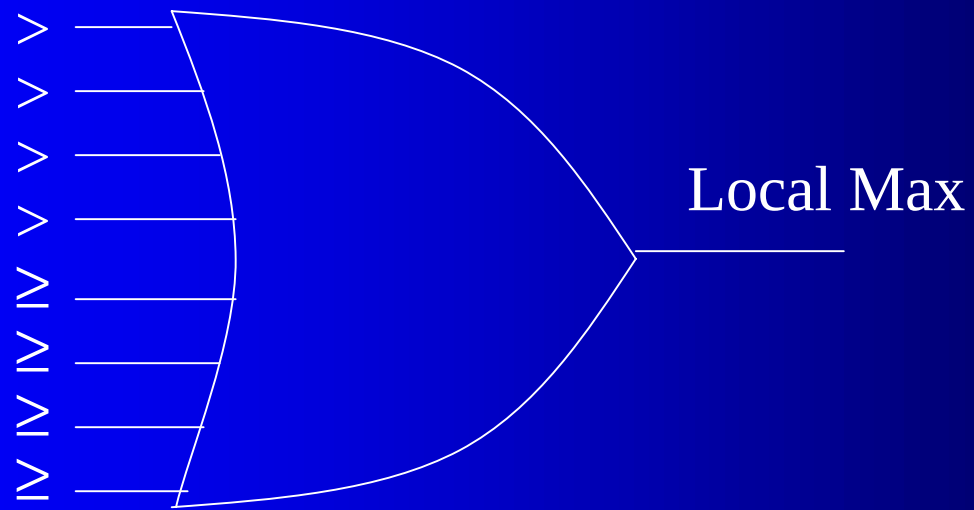
Comparators can be shared



Sam Silverstein:

Local maximum is OR of eight comparisons



Status of algorithm

- Adder trees: completed
- Local maximum ID: completed
- Jet cluster selection: completed
- Threshold comparison: completed
- Level-1, ROI result reporting: nearly done
- Test vector generation: starting to write C++ code

Things left to do

- Finish algorithm
- Synthesize for Virtex - size estimate!
- Simulate and verify with test vectors
- Integrate with rest of algorithm on main processor FPGA
- Produce test vectors for slice tests

Some final words

- We are approaching the point where we need to interface with other work
  - Integration of Jet algorithm on JEM main processor FPGA
  - Testing of algorithm: HDMC?
- Who should Anders and Torbjörn be contacting?