ATLAS
Level-1 Calorimeter Trigger Meeting
RAL 2001

ASIC Labor Heidelberg

PPrASIC Status

History

Layout
- Power pads
- Power routing

Status of the PPrASIC code
- Verilog Logic / Design modifications
- Test environment modifications

Items to be done

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PPrASIC
History

Status at the Mainz meeting:

- Layout (e.g.: manual layout & checks) and timing test were done in parallel.

Layout:

finished a file ready for production at the end of August:

- All layout checks were fulfilled or verified with vendor
- Temperature sensor was powered and function checked

Reviewer of our internal ASIC-Lab Submission-Readiness-Review were not satisfied with:

- Power routing
- Not finished timing test

We decided to change the layout!

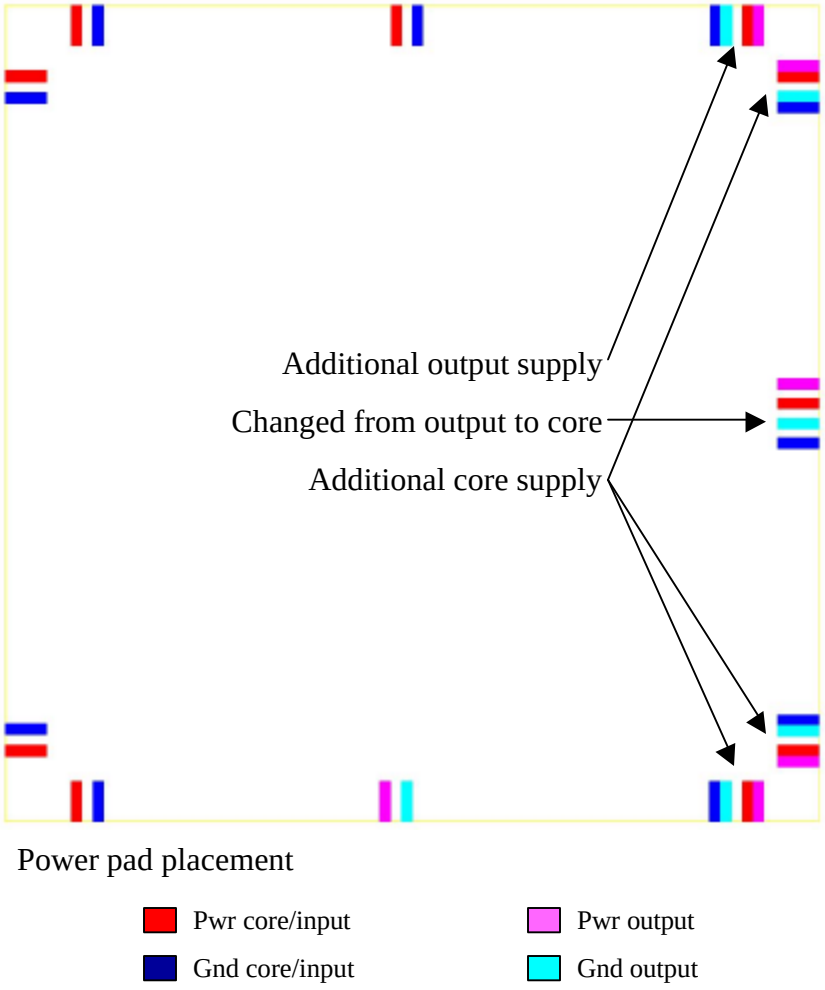
PPrASIC
What has been done

PowerPads

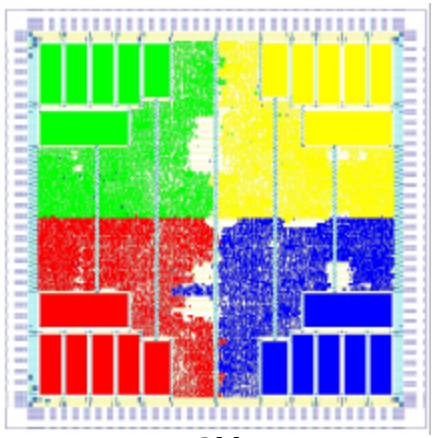
- Chip had 6 pairs of Power pads for core/input supplying max 600mA

- Core needed (toggle rate 40 %) 615,2mA, but also the routing capacitance needed additional 27,4mA.
  The power pads were placed to fit the needs of input and output pads.

- Now 4 additional core supply pads are placed abut to the output driver supply pads.
  => Power for Core is supplied sufficiently symmetrical and the Chip still MCM bondable



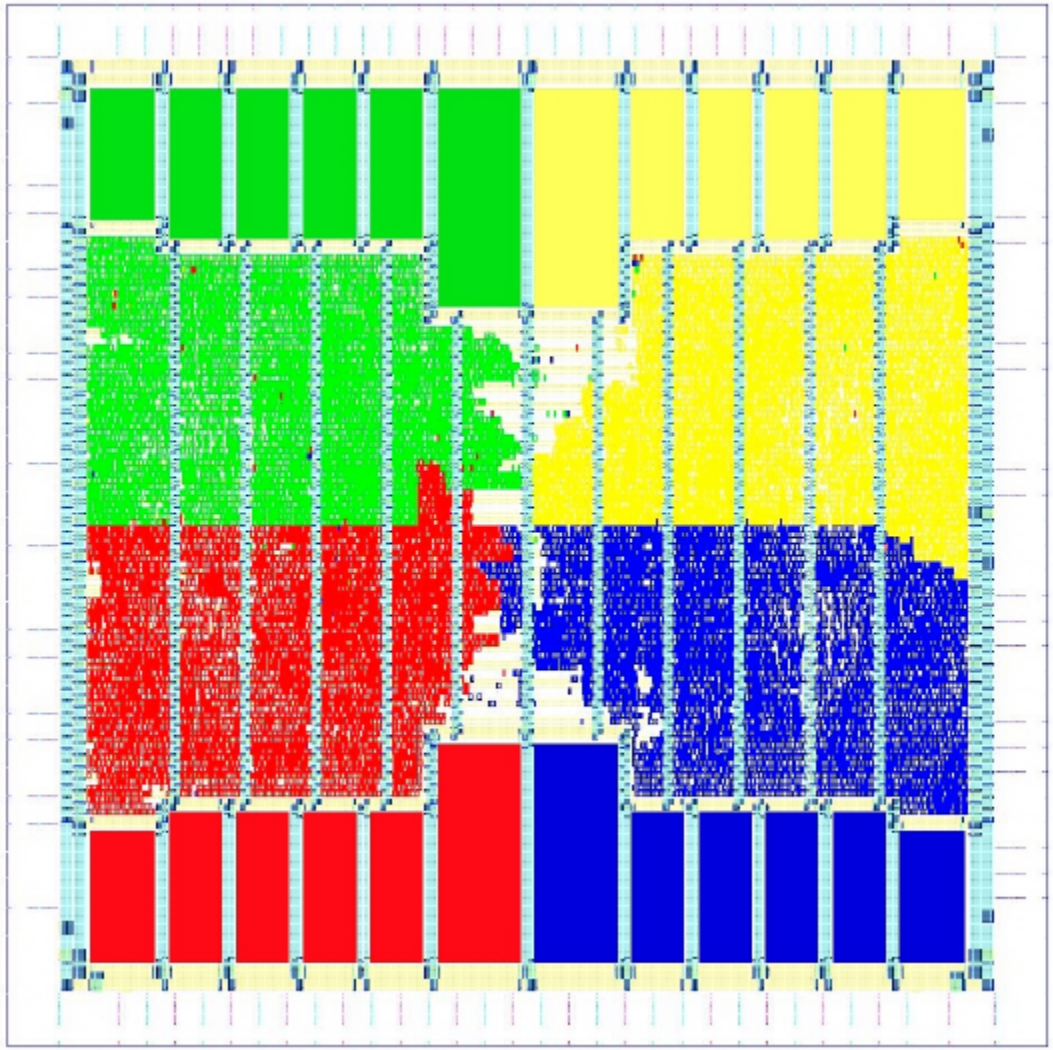
PPrASIC
What has been done



Old power routing

Power routing:

- Ram-Blocks are placed in parallel to optimise the Blockring routing
- The count of power stripes is adapted to the routing of the Blockrings
- Powerring has the same width as the powerpads



New power routing

PPrASIC
Status of the PPrASIC code

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Logical errors detected in verilog code

appropriate modifications / redesign in progress

Verilog Logic / Design modifications:

- BCID decision bits (timing) — corrected!
- Register widths — adjusted!
- Extra register (Sat. BCID algorithm) — added!
- Readout / Derandomizer control — partly done!

Are we sure that the min. number of ticks between 2 L1- Accepts is 4?

Test environment modifications:

- Script generating SerIntface data — corrected!
- Design test module / test benches — extended!

All changes in the verilog code concern Readout and Monitoring only!
No changes to the Realtime Path!

PPrASIC
What has to be done

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Among other items:

- Testing playback and the rest of readout before new synthesis / layout / timing - check
- Updating the CVS repository and documentation
- pre / post layout timing analysis on the netlist!
- Static timing analysis (best / typical / worst cases)

Points to keep in mind:

- Layout problems have been solved
- Most of the timing simulation have been done for the last layout

=> Familiar with design routine => faster iterations

Submission planned at the end of November

Werner Hinderer will give an overview of the testplans.