Overview and Status of the Pre-Processor ReadOUT

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Contents

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- Serial interface of the PPrASIC
- Pre-Processor Module (PPM)
- ReadOut Driver Module (ROD)
- PipelineBus
- VME
- Compression and bandwidth considerations
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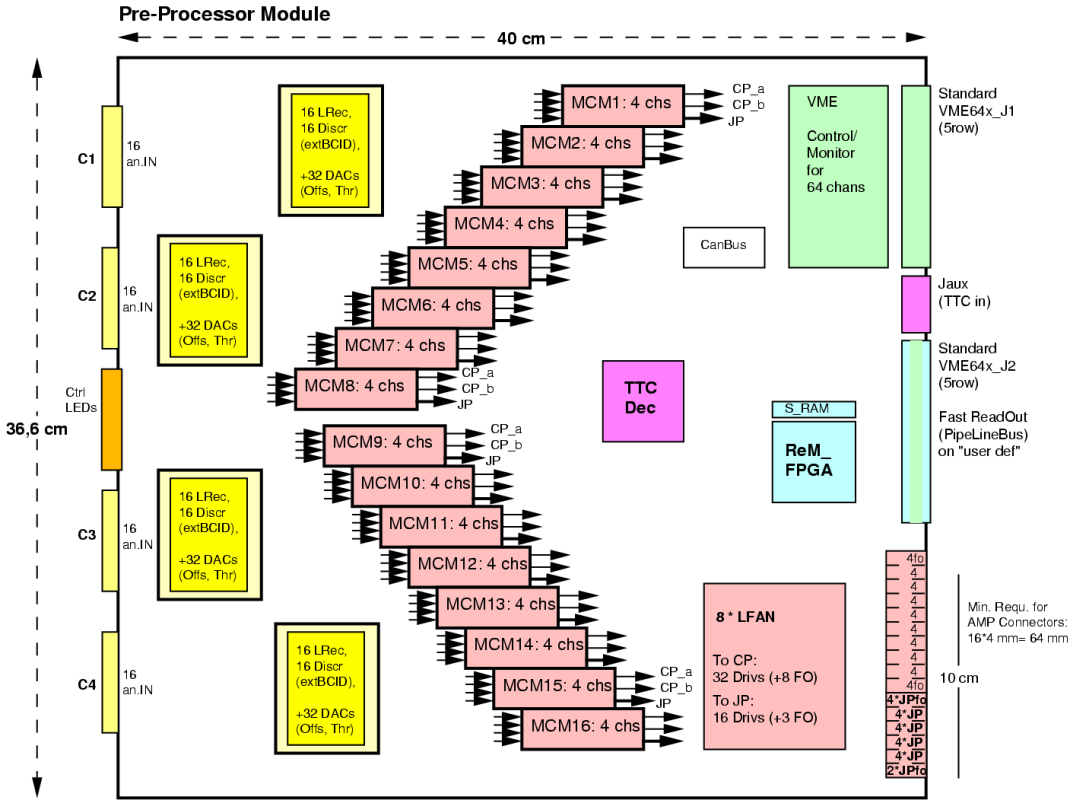
- Q&A...

What am I talking about...



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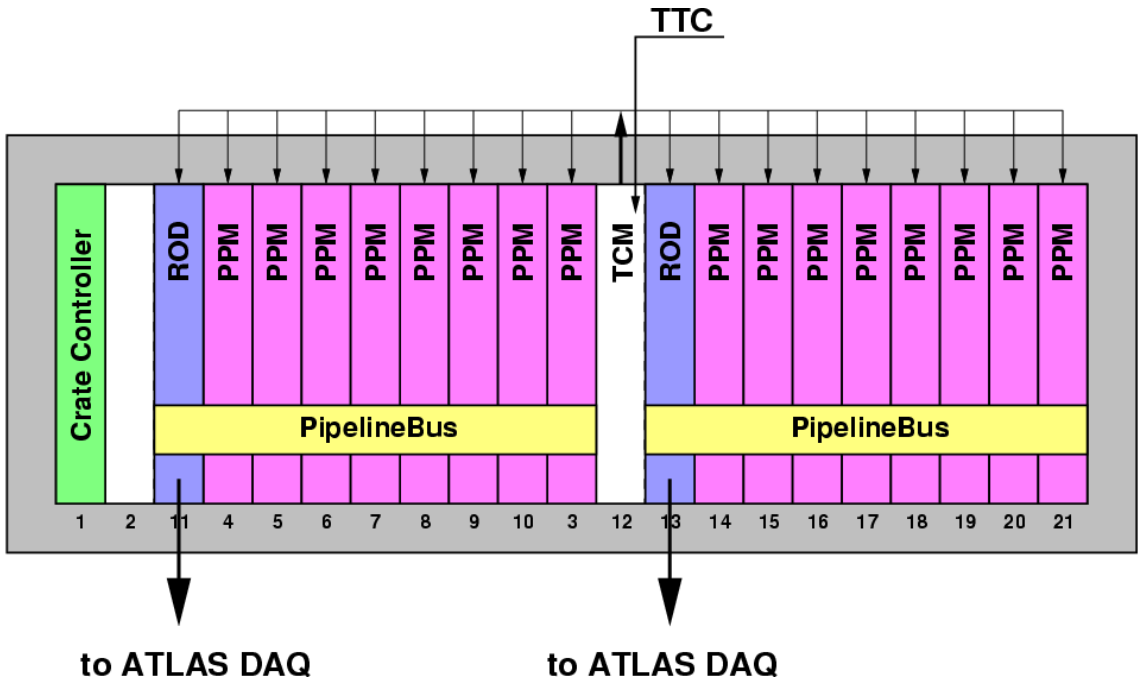

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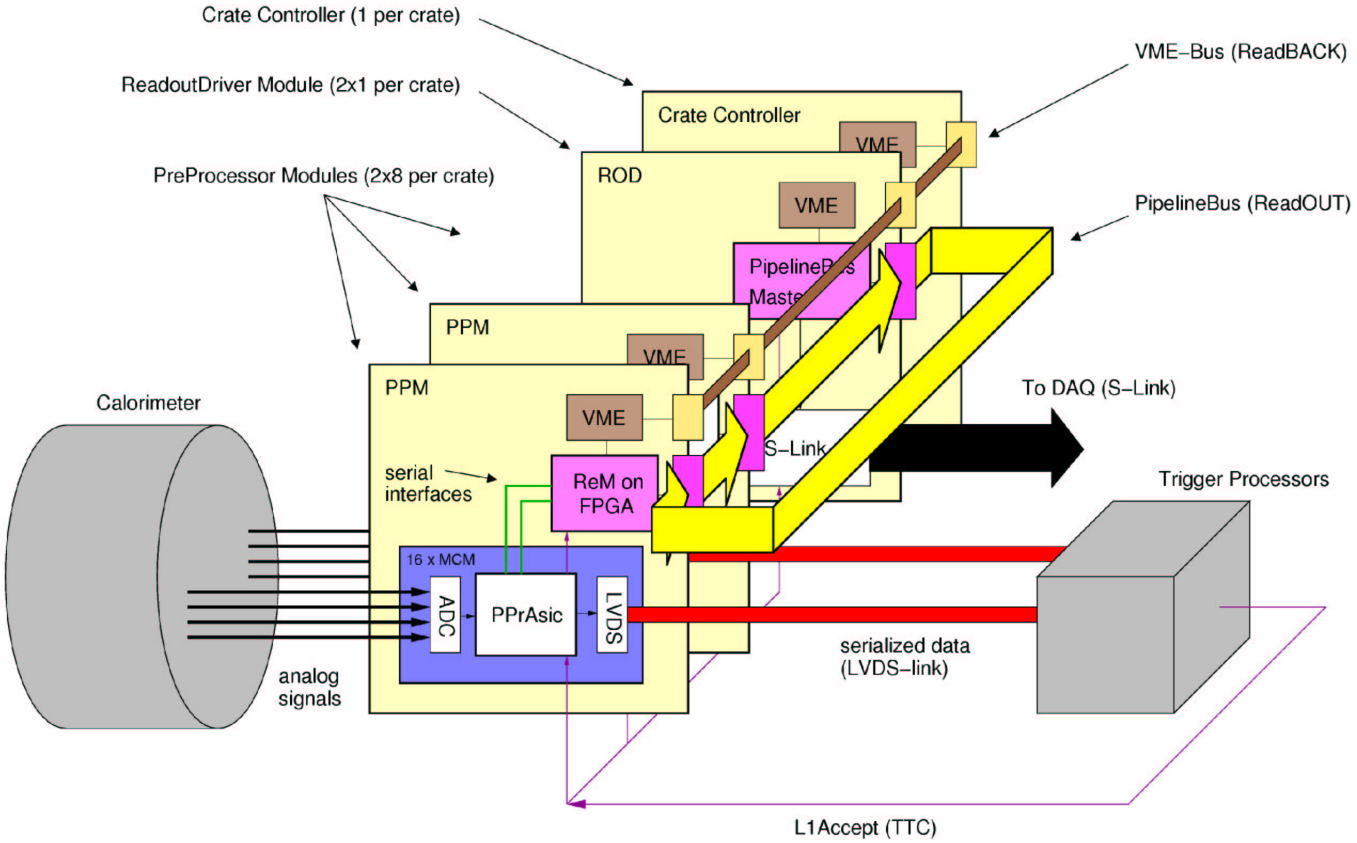
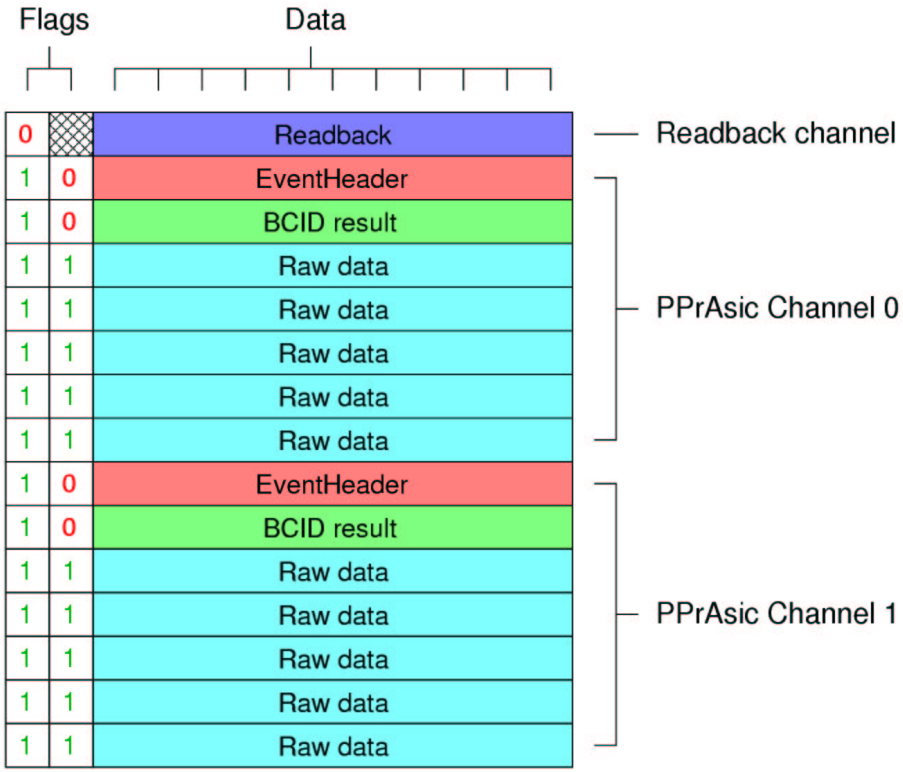


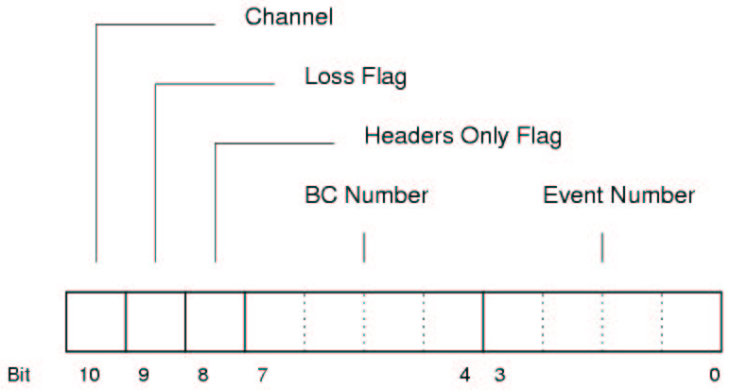
Serial Interface of the PPrASIC

- 16 MCMs with one PPrASIC on each PPM
- PPrASIC has 4 data channels
- PPrASIC has 2 serial interface
- Protocol is a fixed scheme of ReadBACK data and ReadOUT data of 2 channels
- ReadOUT = “real” trigger data
- ReadBACK = memory and registers
- Daisy chaining not an option

Serial Interface of the PPrASIC

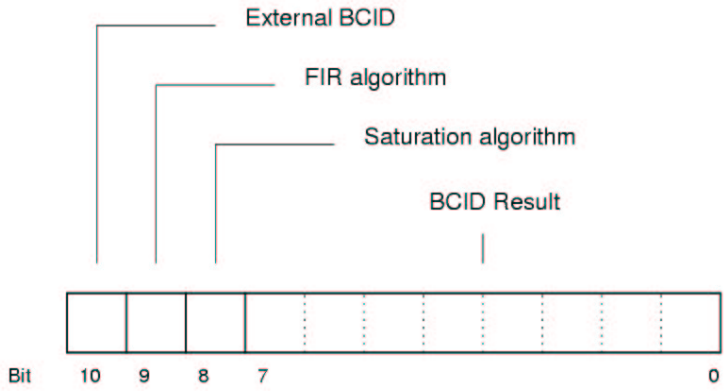


Serial Interface of the PPrASIC ReadOUT – Header



0		Readback
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data

Serial Interface of the PPrASIC ReadOUT – BCID Sample

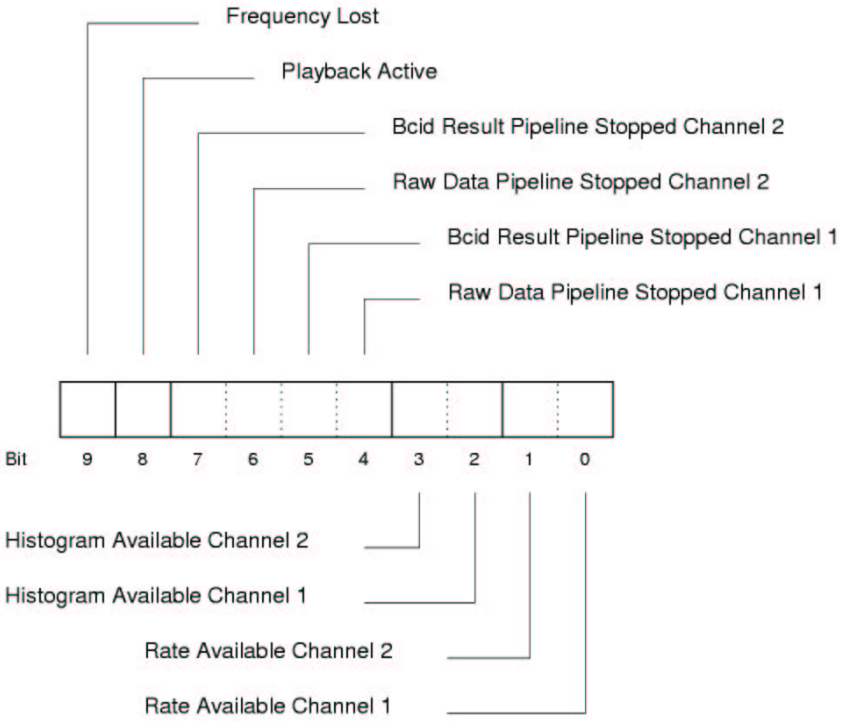


0		Readback
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data

Serial Interface of the PPrASIC ReadOUT – RAW Sample

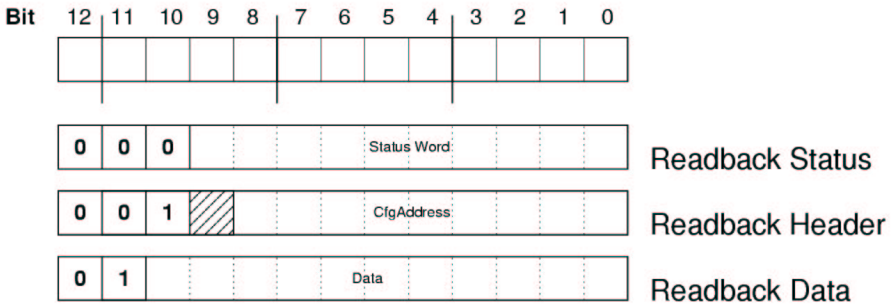
0		Readback
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data

Serial Interface of the PPrASIC ReadBACK – Status Word



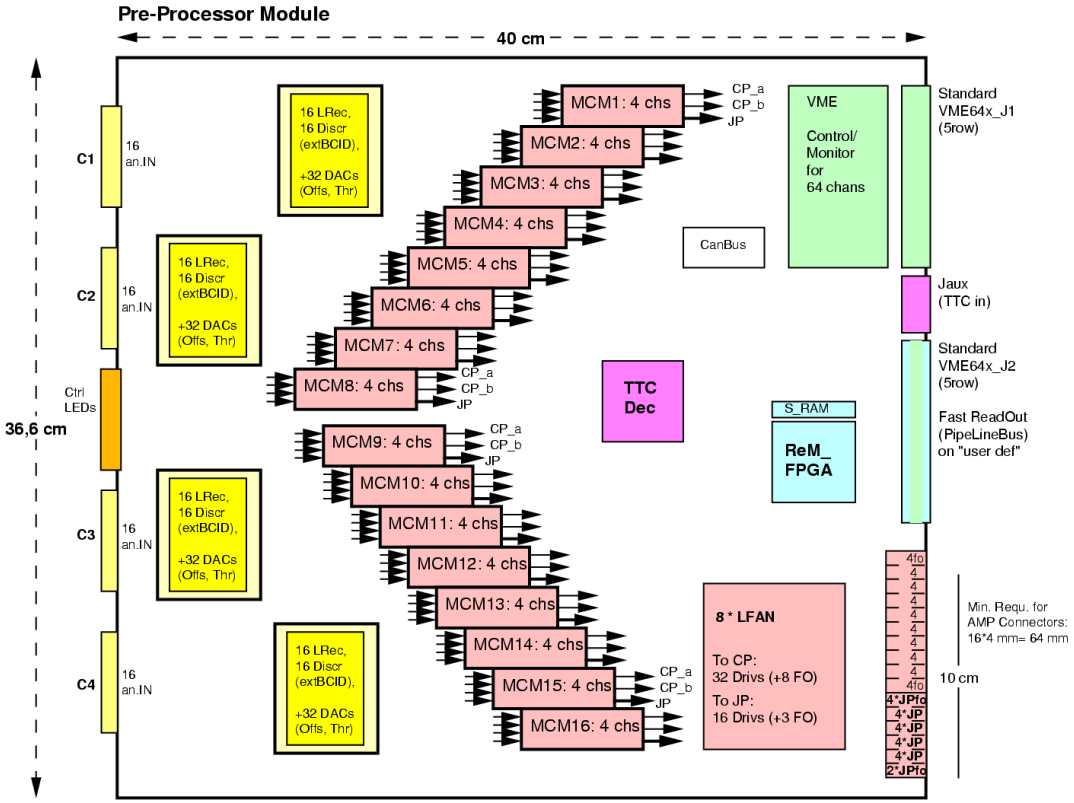
0		Readback
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data

Serial Interface of the PPrASIC
ReadBACK – Format

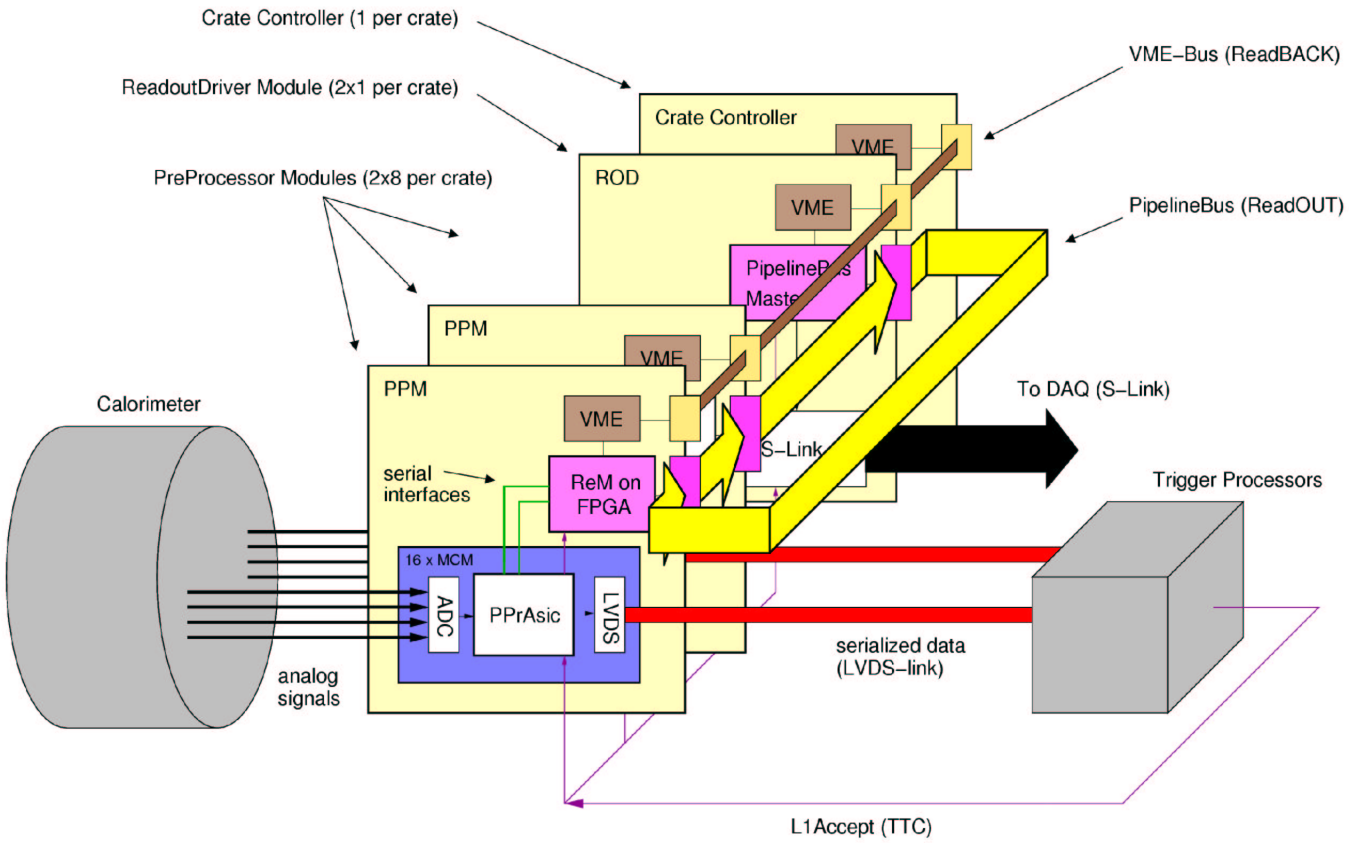


0		Readback
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	0	EventHeader
1	0	BCID result
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data
1	1	Raw data

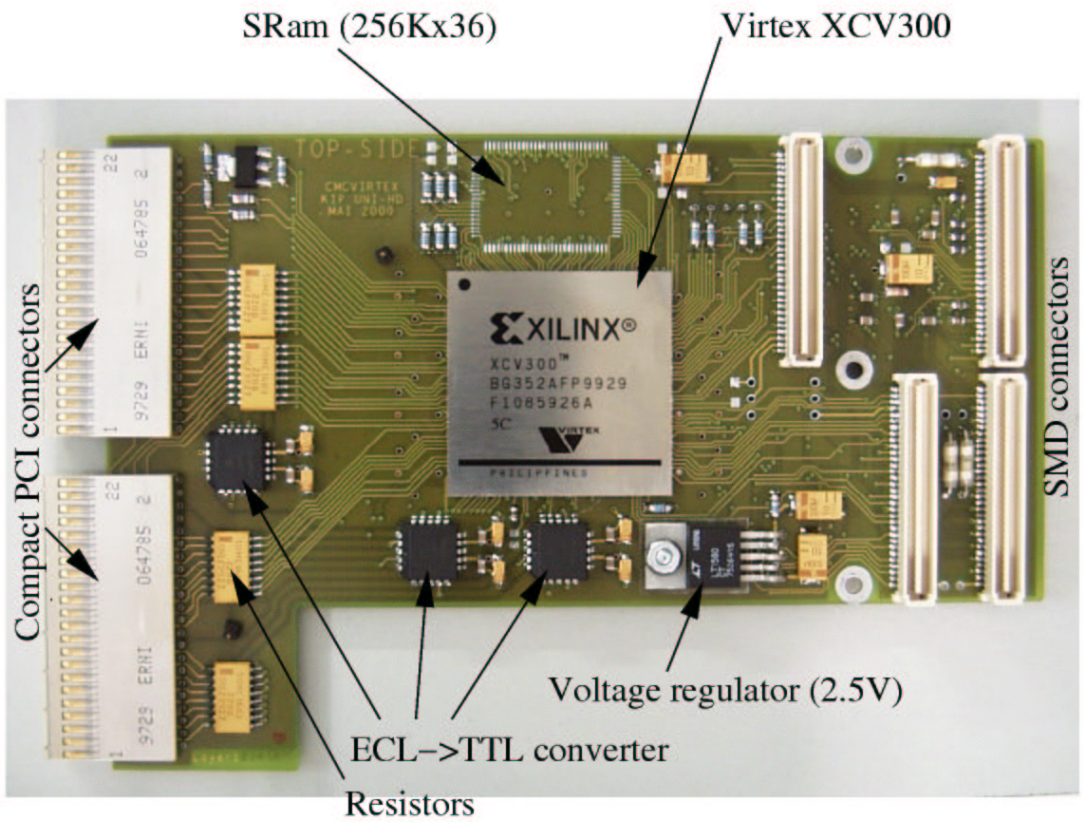
Pre-Processor Module



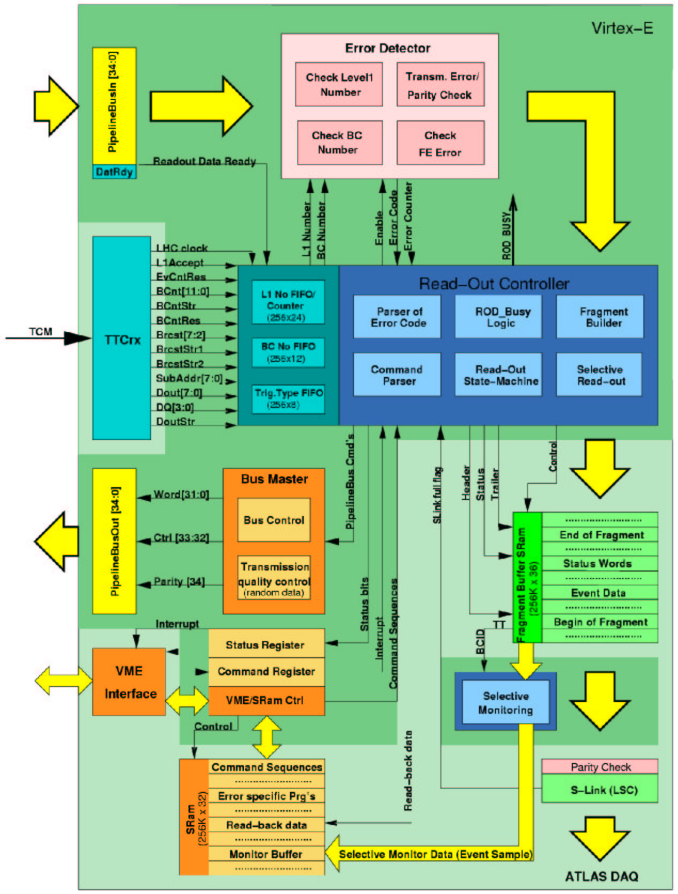
ReadOut-Driver Module (ROD)



ReadOut-Driver Module (ROD)

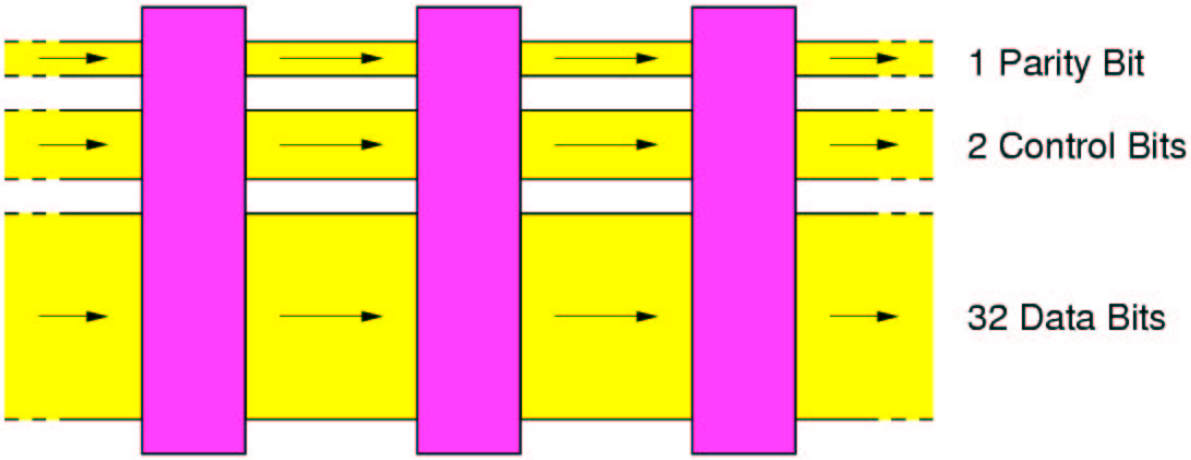


ReadOut-Driver Module (ROD)

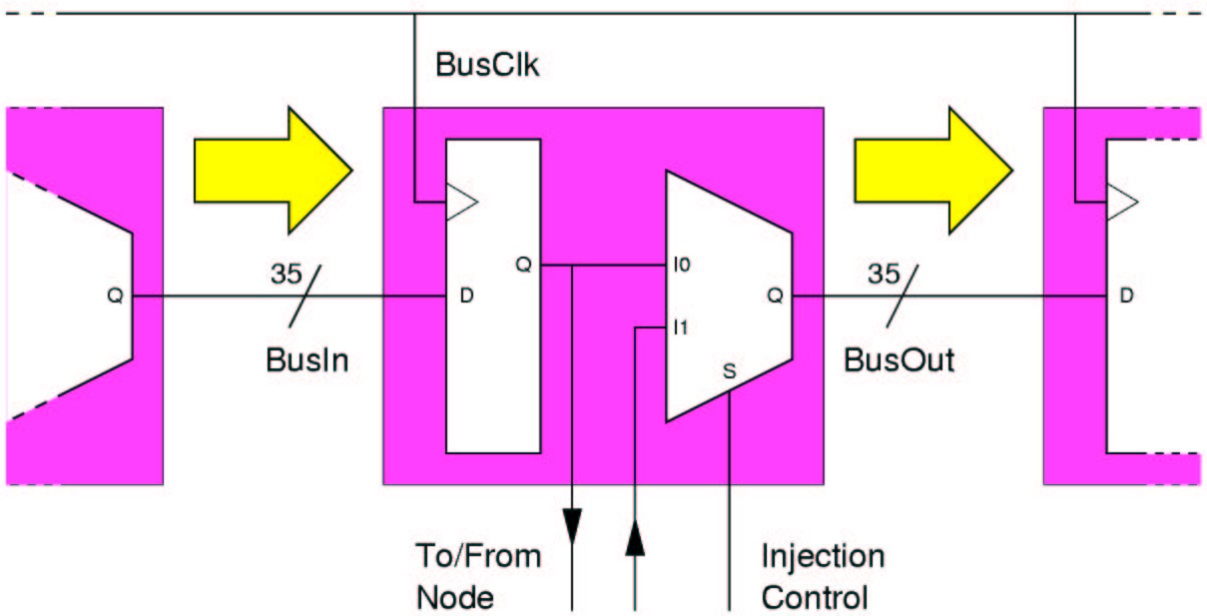


Bernd Stelzer

PipelineBus



PipelineBus



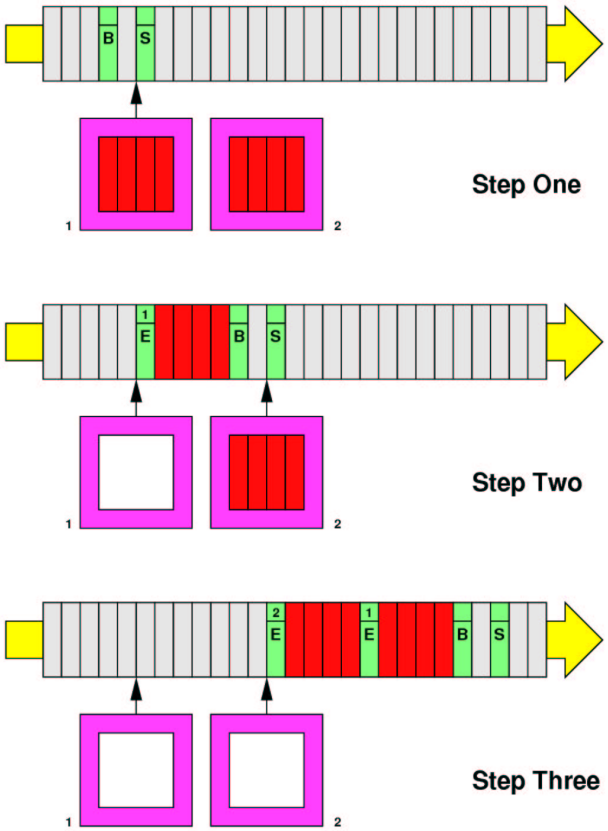
PipelineBus

Empty slot

Command word

Data word

PipelineBus



VME Interface

- VME and PipelineBus offer the same commands and functionality
- Too slow for ReadOUT data
- Suitable for ReadBACK (e.g. histogramm)
- Suitable for configuration
- Suitable for testing of one PPM

Bandwidth and compression

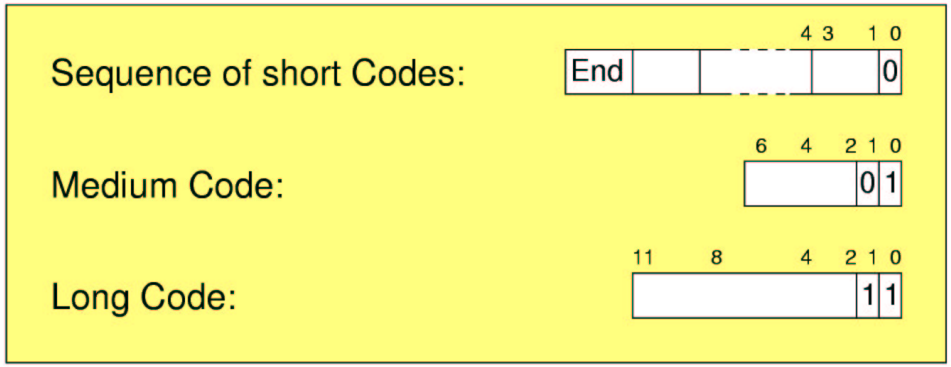
- 100kHz (75kHz) L1-Accept rate
- 1 BCID sample per channel (8+3 Bits)
- 5 (3) RAW samples per channel (10+1)
- Flag bits per channel (5 – 13 Bits)
- Flag bits per PPM (8 - 16 Bits)
- PipelineBus commands and idle cycles

Bandwidth and compression

Data type	Bits	Multiplier	Total Bits	Compress	MB/s	MB/s
BCID Sample	8	512	4096	1	48.83	48.83
BCID Algorithm	3	512	1536	1	18.31	18.31
RAW Sample	50	512	25600	2.2	305.18	138.72
RAW Ext BCID	5	512	2560	1	30.52	30.52
Flags (per channel)	5	512	2560	1	30.52	30.52
Flags (per PPM)	9	8	72	1	0.86	0.86
PBus (per PPM)	32	8	256	1	3.05	3.05
PBus (per ROD)	384	1	384	1	4.58	4.58
Data rate: 100 kHz			**37064**	**1.6**	**441.84**	**275.38**

- **100 kHz L1-accept rate**
  - 1:5 → 275.38 MB/s
  - 1:3 → 207.68 MB/s
  - 1:0 → 106.14 MB/s
- **75 kHz L1-accept rate**
  - 1:5 → 206.53 MB/s
  - 1:3 → 155.76 MB/s
  - 1:0 → 79.61 MB/s

Bandwidth and compression Quality of Algorithms



Absolute algorithm			
Pedestal →	0	5	10
Noise mean deviation ↓			
2	2.84	2.52	1.74
4	2.80	2.43	1.86
6	2.74	2.39	1.94

Difference algorithm			
Pedestal →	0	5	10
Noise mean deviation ↓			
2	2.62	2.34	2.22
4	2.52	2.15	2.01
6	2.41	2.05	1.88

Volker Schatz

Bandwidth and compression Consequences

- PipelineBus
  - 40MHz → 160MB/s
  - **60MHz → 240MB/s**
  - 80MHz → 320MB/s
- ROD
  - Data rate doubled → FPGA speed issues ?
- S-LINKs
  - Two double-rate links needed (2x 128MB/s)
  - Consequences for DAQ (storage, speed, etc.) ?

Bandwidth and compression “Deprecated illusions”

Data type	Bits	Multiplier	Total Bits	Compress	MB/s	MB/s
BCID Sample	8	512	4096	2.5	48.83	19.53
BCID Algorithm	0	512	0	2.5	0	0
RAW Sample	50	512	25600	2.5	305.18	122.07
RAW Ext BCID	0	512	0	2.5	0	0
Flags (per channel)	0	512	0	2.5	0	0
Flags (per PPM)	0	8	0	2.5	0	0
PBus (per PPM)	0	8	0	1	0	0
PBus (per ROD)	320	1	320	1	3.81	3.81
Data rate: 100 kHz			**30016**	**2.46**	**357.82**	**145.42**

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Data rate: 100 kHz			**37064**	**1.6**	**441.84**	**275.38**

State of RemFPGA verilog code

- Serial interface - done
- I²C-Bus - done
- PipelineBus - done
- Compression & error check - partly
- Control logic, registers, etc. - partly
- VME Interface - not done
- Testing of code - hardly

Conclusions

- (1 BCID : 5 RAW) not possible at L1-rate of 100kHz
- (1:3) at 100kHz or (1:5) at 75kHz is ok
- ROD FPGA code needs to be adjusted, but not completely rewritten
- No ROD/DAQ-“event format” has been designed yet
- Existing hardware (Virtex300) can be used for slice test (speed is not an issue: only 2 PPMs)
- Need info of “noise performance” of the detector
- Question: “fast 32-Bit barrel-shifter with Virtex”

Questions & Answers