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Readout Issues and TDAQ.

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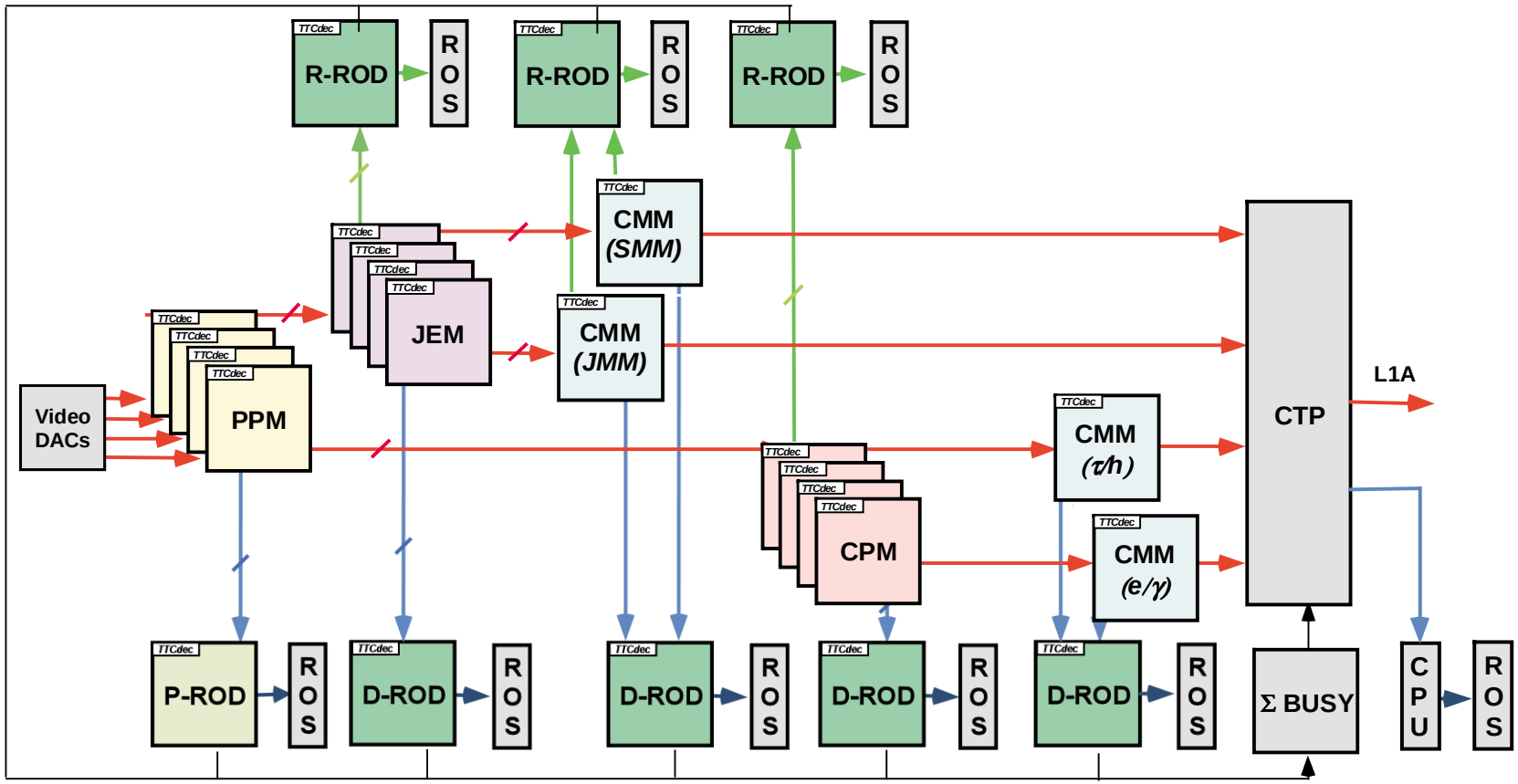
Components of Slice Test



CTPD: Triggering & Readout

- **Triggering**
  - Start with TTC only, but use CTPD later as timing alters.
  - hard to control system if L1A from CTPD is generated by garbled hits from CMM when debugging the system.
  - therefore (at least initially) enable only 1 input bit to generate L1A, but still read out all 32 bits - of which say 30 from CMMs.
- **Readout**
  - timeslices go into a FIFO on the CTPD. There is enough room for ~ 2k 4-word timeslices.
  - Each event generates 1 to 5 timeslices (programmable).
  - A CPU with S-Link mezzanine must read, build, and send event fragments.

CMM: Hit Outputs

- **CMMs together generate 98 data bits and 5 parity bits. Only 30 can be read by the CTPD.**
- **To read all the bits when the system is being driven from the PPr video memory requires special firmware in two DSS modules plus extra software and an extra S-link**
  - capture timeslices in DSS when L1A is received, then read both DSS modules by crate CPU and send as an S-link fragment.
- **Propose instead to rely on slice readout from the merger modules.**
  - With separate tests to ensure that this is equivalent.
  - This needs the extra firmware & software but not an extra S-link

Strategy

- **Separate tests of groups of modules April-June 2002**
  - UK - e/γ + τ/h processor:
    - ***CPM, CMM, D-ROD, R-ROD, TCM, VMM , Backplane (+ DSS,GTM)***
  - Heidelberg - Preprocessor
    - ***PPM, P-ROD, TCM, (VideoDac)***
  - Mainz - Jet/Energy-Sum processor (partly done in Heidelberg?)
    - ***JEM, CMM, D-ROD, R-ROD, TCM, VMM, Backplane***
  - CERN - Central Trigger processor
    - ***CTPD, (Patch panel)***
- **Full tests in Heidelberg**
  - starting June 2002, order depends on institute test completion
  - Underlined Module names indicate full-specification prototypes

Types of Test

- **Subsystem tests should fully test individual modules and module sets before incorporation into the full slice test.**
  - Iterate over large range of test vectors to explore performance.
  - Check algorithms
- **The full slice test should concentrate on system aspects**
  - Reliability, link purity, error handling…
  - Timing issues - common timing windows, overall latency, system stability, all modules using TTC.
  - Software issues - hopefully all components fully integrated in a software system prototype

Software !

- **We need various components to run our hardware during tests. We are developing a prototype framework to bring them together:**
  - Test spec - Input vector generator - Simulation -> Test Vectors - managing sequences of vectors - event analysis - ROS
  - HDMC module definitions - module classes - system control - Online software.
  - Algorithm thresholds - trigger menus - database
  - etc.

Questions for Ourselves

- **How do we check that the links are error-free to 1 bit in 10^{10} .**
  - Long data analysis runs comparing sent and received data after readout (software), or use DSS modules (hardware), or use parity indicators. (Can PPr send wrong parity?)
- **We must run at 100 kHz L1A to check that the system works. Can we use short bursts of events or must it be sustained rate?**
  - Data rate at 100kHz is ~400 Mbytes/sec total on 9 S-Links.
  - The ROS PC will not have the PCI bandwidth or CPU power to handle (read, build, monitor) events at 100 kHz. So we need ROBINs for sustained 100kHz running.
  - At 1kHz sampling rate (guess), can sample 3.6 x 10^6 events/hour.

S-Link: Numbers and Data Rates (1)

Source	Slinks	Data rate (Mb/s)
PPrs via PPROD	1	*100 (estimate)*
CPM Slice (4 G-Links)	1	137.2
CPM RoI (4 G-Links)	1	12.4
JEM Slice (4 G-Links)	1	*86.0 (estimate)*
JEM RoI (4 G-Links)	1	12.4
CMM Slice (2 CP, 1 Jet, 1 Esum G-links)	2	*22 (estimate)*
CMM RoI (1 G-Link via CPROD)	1	12.4
CTPD via RIO CPU	1	7.6
TOTAL	**9**	**390.0**

S-Link: Numbers and Data Rates (2)

- **Assumptions:**
  - 100kHz L1A,
  - read one timeslice per L1A with or without zero suppression
  - 16 RoIs per event;
  - 4 words of data from CTPD copied directly to event fragment;
- **How to connect 9 S-Links to a PC**
  - S-Link to PCI interfaces or ROBIN boards.
  - use PCI expansion crate as only 3 PCI slots are available
  - link to the PC PCI by around 1m of cable.
  - Up to 13 slots can be added. Claimed speeds up to 132 Mbytes/sec.

Requirements (1)

- **Read out one or a few modules at low and moderate rates for debugging. The system must stay alive when faults occur.**
- **Run at 100 kHz to check LVDS links (40 MHz).**
  - Check links with parity counters
- **Run at 100 kHz (burst?) to soak test individual modules & small module chains.**
  - analysing a subset of events.
  - Or analysing all events in burst. RODs need lots of memory.
- **Software can check only a subset of events**
  - 20 kHz checking of RoI packets during the ROD integration test.
  - At 1kHz (guess), a 1 hour run samples 3.6 million events.

Requirements (2)

- **Do we need more sensitivity than this?**
  - If so, we need to use DSS checking. It won't work with data from the video memories
  - But it is Hard to select events for computer checking or display based on DSS results.
- **There are two possible schemes for sustained 100kHz running:**
  - using a ROD-crate DAQ system, sample events in the RODs.
  - use a ROS system. ROBIN modules are required to receive the events, and a subset are selected and analysed à la level-2..
- **Both schemes need software development. The ROS scheme (this talk) is similar to the one used in the Atlas test beam DAQ.**

Access to ROBINs

- The ROS PC will not have the PCI bandwidth or CPU power to handle (read, build, monitor) events at 100 kHz.
- ROBIN modules receive fragments and buffer them, and expect software messages to delete or read out each event.
- RHUL is building ROBIN modules with ODIN-compatible input. We need one ROBIN for each S-Link (total 8).
  - ***supporting software and firmware to run on the ROBIN modules;***
  - ***supporting software in the ROS PC.***
- The slice test will use the ROBINs at a sustained 100kHz rate. This should be done in the UK in the first to check that it works.

How to Run

- Trigger using TTC
- Transmit Slice and RoI data over S-Links to ROBIN boards in a suitable PC running the ROS software.
- Use the TRG or Level-2 component of the ROS to pre-select a subset of events for event-building in the PC. Rejected events are deleted in the ROBINs.
- Build then distribute events to the event factory, for sampling by monitoring programs using the online monitoring skeleton.
- Histograms, if required, will be provided via T. Shah's ROOT software unless an alternative is available from Atlas.

End

The End