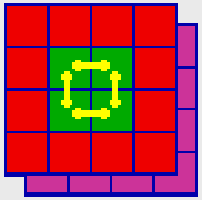

ATLAS Level-1
Calorimeter Trigger



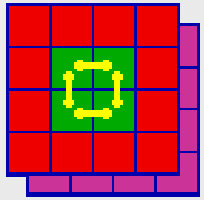
# CP/JEP ROD Prototype Test Status

## Infinite and countable?

B.M. Barnett, Rutherford Appleton Laboratory

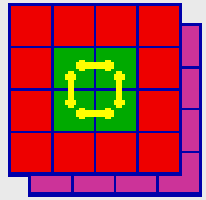
Collaboration Meeting. November 7-10, 2001

# Overview



- Mandate
- Test Setups (2)
- Fault Status
- Keeping Track of the Fixes
- Where next?

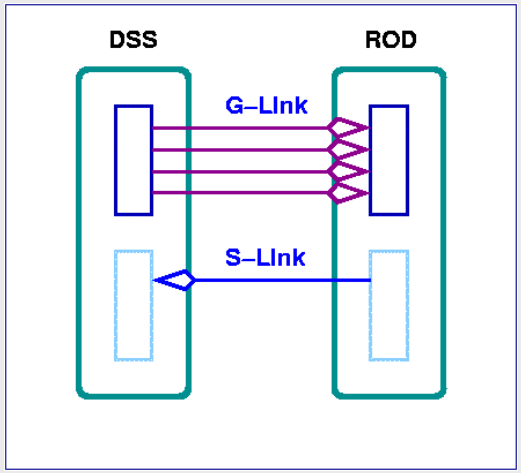
# Mandate

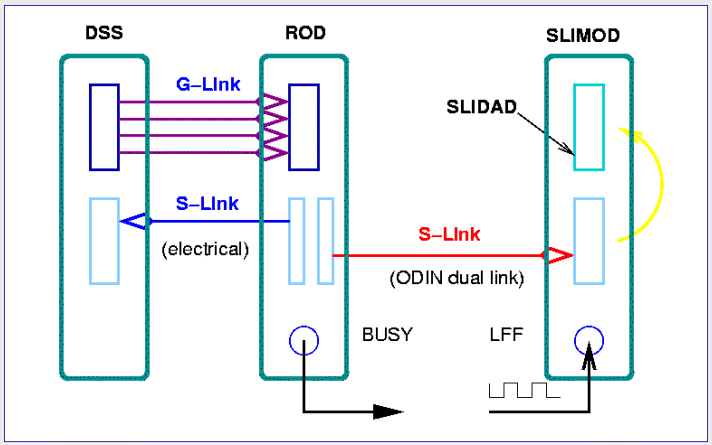


- Test CP/JEP ROD functionality
  - CP Mode. Slice and RoI.
  - in absence of external interfaces (standalone)
    - emulate CPM (input) and ROS/RoiBuilder (output) using Data Source Sink Module (DSS)
  - in conjunction with external interfaces
    - emulate CPM (input) with DSS
    - at CERN with RoIBuilder
    - with ROS Frontend at RAL

# Test Setups (1/2)

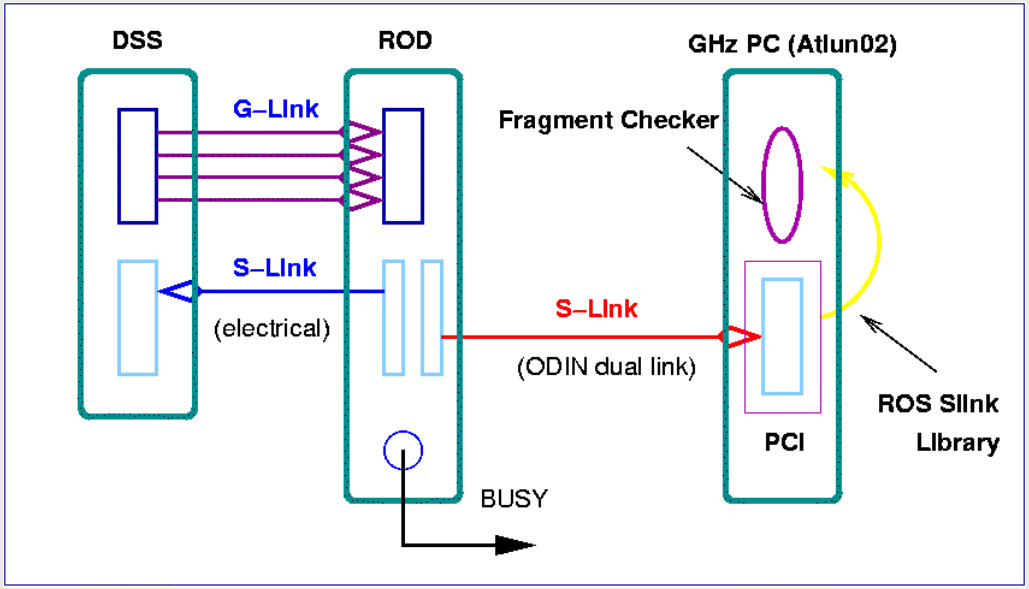
- Standalone Behaviour
- Events:
  - Vectors pre-loaded in DSS G-link output buffer
  - L1As in bursts distributed through TTC system
  - Either:
    - fast flow (no XOFF)
    - regulated flow



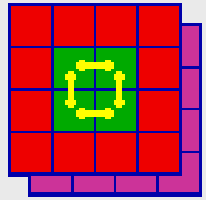



# Test Setups (2/2)

- Conformance at the interface.
- Test for FIFO empty failure
  - due to flow control
  - LFF driven by ODIN

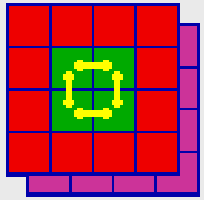


# Fault Status



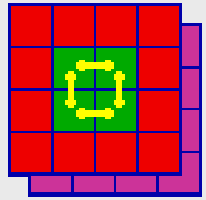
| Fault | Description | Status |
|---|---|---|
| **DSS-1** | S-link destination address counter miscount | Await fix |
| **DSS-2** | DAV Glitch | Requires study |
| **DSS-3** | Slice value of 4,5 not interpreted correctly | Done |
| **CPSlice-1** | *CPM-ROD link down on FPGA/TT= 01000/11* | Fix awaits test |
| **CPSlice-2** | Substatus Word misnumbering. | Done |
| **CPRoI-3** | FIFO doesn't empty (Flow control fails) | Done |
| **CPRoI-4** | Channel/Module ID Bits swapped | Done |
| **CPRoI-5** | BOF in S-Link record seen as BOF00001 | s/w artifact |
| **CPSlice-6** | S-link LFF enable mask and s/w XOFF have no effect. (Slice operation) | Done |
| **CPSlice-7** | Slice readout modes with more than one slice fail. | Done |
| **CPSlice-8**. | Bad Sub-status words in multi-slice operation | Done |
| **CPRoI-9** | Spy buffer registers clear doesn’t work | Await Fix |
| **CPSlice-10** | Operation fails after initial fragment | Done |
| **CPSlice-11** | Parity Error word incorrect | Done |

# Keeping Track of the Fixes



- Viraj:
  - "I have revisited the QA procedures on how to record the problems and their fixes encountered during module commissioning and testing.
  - There are two form we can use:
    1. Route Card, this will be for recording module specific problems and fixes during initial inspection, testing and operational phase.
    2. Problem Report, (see attached example) to record common design problems and solutions. I believe this will be the appropriate form to use for firmware problems."

# Where Next?



- There is convergence in firmware debugging
- Now, on to the last fix (or is it two ...)
- Test zero suppression thoroughly (RoI/Slice)
- Soak tests (the hard stuff)
  - some errors observed at level of a few per 10,000,000
- Comprehensive test vectors.
- DSS modifications:
  - hardware fragment check
  - wraparound (cycle without s/w intervention.)