#### Introduction

#### Adam Davis Electronics System Support

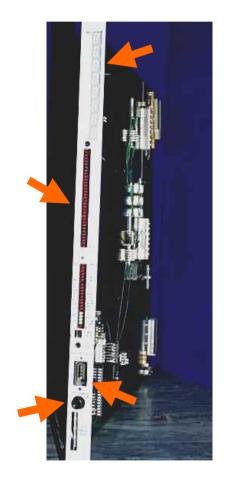
# Layout of Talk

- What is the TCM?
- Problems with the TCM
- Status of the TCM
- Decisions we made
- Where we are now
- Further testing problems
- Future ALC Designs Considerations

# What is the TCM

9U Module
VME Hex Display
VME LED Display
TTC

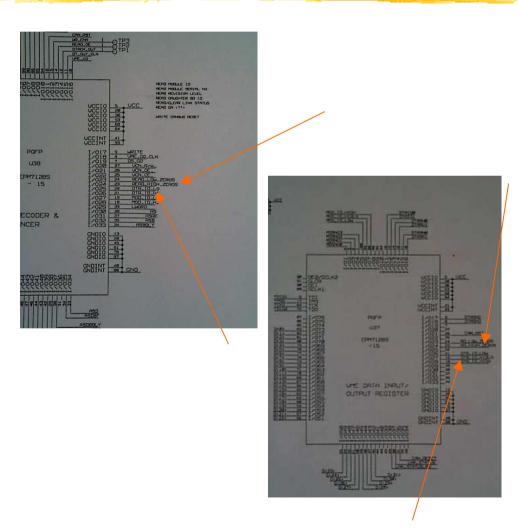
CAN Bus



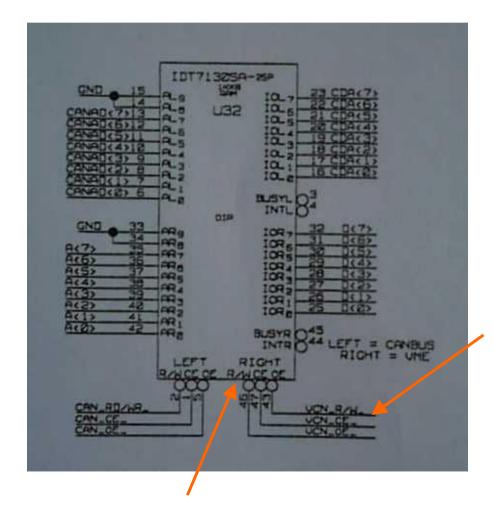
- Connector
  - Incorrect wiring (Write\*)
- VME Decoder
  - Net Names
  - Firmware(adddec)
- Register Decoder
  - Net Names
  - Firmware(en2reg)

- Dual Port Memory
  - Net names
  - Timing problems
- Hex Display
  - Firmware
  - Timing problems

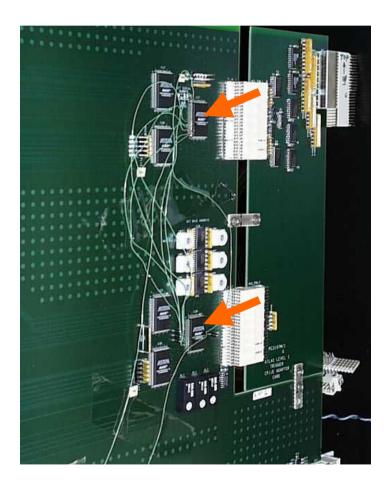
Schematic
READ\_HIGH\_ZEROS
RD\_HIGH\_ZEROS
DTR\_ID\_HI
DTR\_ID\_HIGH



# Nets mixed up VCN\_R/W VCN\_OE\_

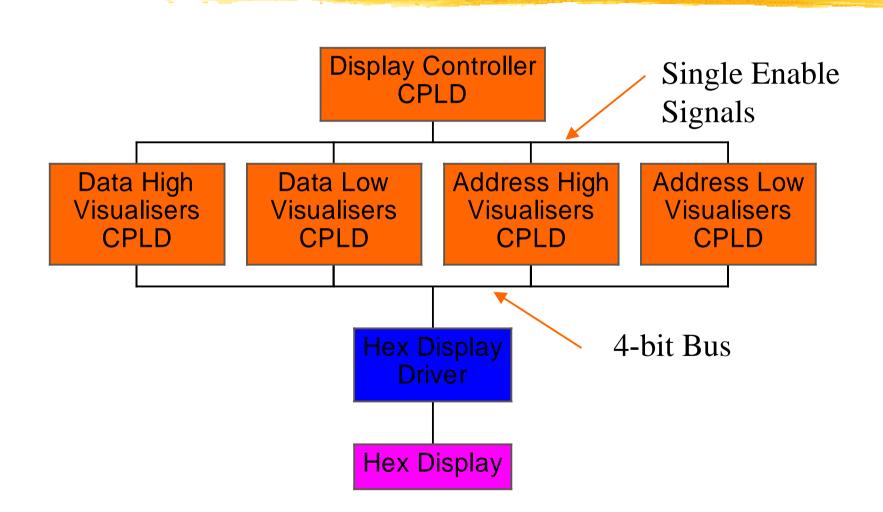


- 9 Wire ModificationsVME Decoder
- Register Decoder

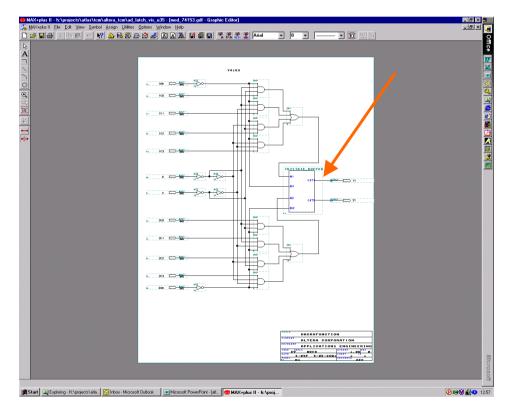


Could these errors been avoided.?

- Check schematic
- Check net list
- Check again
- Is there a way of checking the net list automatically.? Yes there is...



#### Tri\_state buffer



TITLE "tristate_buffer";	
SUBDESIGN tristate_buffer (	
IN1, IN2, En1, En2 OUT1, OUT2 )	:INPUT; :BIDIR;
VARIABLE	
OUT1_TNODE, OUT2_TNODE	:TRI_STATE_NODE;
BEGIN	
OUT1_TNODE = TRI(IN 1, En 1); OUT1 = OUT1_TNODE;	
OUT2_TNODE = TRI(IN2, En2); OUT2 = OUT2_TNODE;	
END;	

. . . . . .

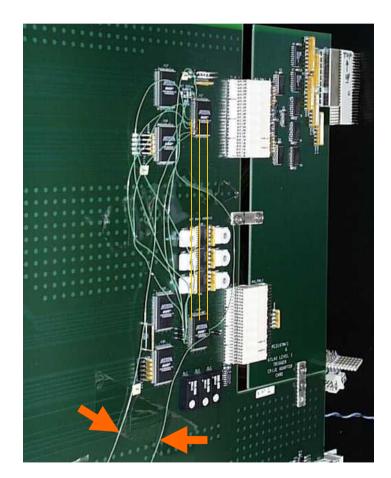
# **Status of the TCM**

- Read Module ID Code "3195"
- Read Module Serial Number
- Read Daughter Serial Number
- CAN Micro controller Reset

# **Status of the TCM**

- Write to DPM
- Read from DPM
- "Hex display" display's Address
- "Hex display" display's Data
- LED's Display correct Data + Address

- Do we need to make these modifications?
- Yes, but only two of them (link status)
- Use three enable signals for address decoding and eliminate 7 wire modifications.



Or, we could make the boards again taking into account the required modifications but keeping the original(ish) CPLD design.

#### Change CPLD Design

- Keep and use boards already made(7) - 3 populated
- New boards will have more recourses, allowing for expansion of design
- Modify Boards
- Don't spend time modifying CPLD design
- Easier to debug
- Using design to full extent and as it was originally intended

Recommendations

- Redesign the CPLD's
- 6 boards only need wire 2 modifications
- New boards with modifications increasing recourses if necessary

<pre>Add provide the set of the s</pre>	E I I I I I I I I I I I I I I I I I I I
<pre>TITLE "Read Write Strobes"; SUBDESIGN rd_wr_strobes_mod ( read, write, lword : INPUT; a[70] : INPUT; addr_ok : INPUT; mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_lo_strop : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; lo = TRI(0,GND); mod_id_lo = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"00000100" =&gt; 0,0,1; 1,1,8"00000100" =&gt; 0,1,1; 1,8"00000100" =&gt; 0,1,1; 1,8"00000100" =&gt; 1,0,0; 1,1,8"00000100" =&gt; 1,0,1; 1,0,8"00000100" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"001xxxxx" =&gt; 0; dtr_ok, a[70] =&gt; dpmem_en_; dtr_ok, a[70] =&gt; dpmem_en_; dt</pre>	Fixedsys 10 10 E E E
<pre>SUBDESIGN rd_wr_strobes_mod ( read, write, lword : INPUT; a[70] : INPUT; addr_ok : INPUT; addr_ok : INPUT; mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; dpmem_en_ : OUTPUT; dpmem_en_ : OUTPUT; dpmem_en_ : OUTPUT; dpmem_en_ : OUTPUT; dfr_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); tdr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"0000000" =&gt; 0,10; 1,1,8"0000010" =&gt; 0,10; 1,1,8"0000010" =&gt; 1,0,0; 1,1,8"0000010" =&gt; 1,0,0; 1,1,8"0000010" =&gt; 1,0,1; 1,0,8"0000110" =&gt; 1,1,1; 0,x,8"xxxxxxx" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"0010Xxxxx" =&gt; 0; dot_ok, a[70] =&gt; dpmem_en_; 1, 8"0010Xxxxx" =&gt; 0; dot_ok, a[70] =&gt; dpmem_en_; 1, 8"00Xxxxx" =&gt; 0; dot_ck, a[70] =&gt; dpmem_en_; 1, 8"0Xxxxxx" =&gt; 0; dot_ck, a[70] =&gt; dpmem_en_; dot_ck, a[70] =&gt;</pre>	
<pre>(     read, write, lword : INPUT;     a[70] : INPUT;     addr_ok : INPUT;     addr_ok : INPUT;     mod_id_lo, mod_id_hi : BIDIR;     mod_id_lo, dtr_id_hi : BIDIR;     mod_id_lo, dtr_id_hi : BIDIR;     dtr_id_hi2lo : OUTPUT;     read_high_zeros, read_low_zeros : BIDIR;     can_rst : OUTPUT;     dpmem_en_ : OUTPUT;     dff = TRI(0,GND);     mod_id_lo = TRI(0,GND);     read_low_zeros = TRI(0,GND);     tread_low_zeros = TRI(0,GND);     tread_low_zeros = TRI(0,GND);     tRBLE     addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst;     1,1,8"00000000" =&gt; 0,1,0;     1,1,8"0000010" =&gt; 1,0,0;     1,1,8"0000010" =&gt; 1,0,0;     1,1,8"00001100" =&gt; 1,0,0;     1,1,8"00001100" =&gt; 1,1,1;     0,x,8"xxxxxxx" =&gt; 0,0;     extract = 0;     extract =&gt; 0;     extr</pre>	
<pre>(     read, write, lword : INPUT;     a[70] : INPUT;     addr_ok : INPUT;     addr_ok : INPUT;     mod_id_lo, mod_id_hi : BIDIR;     mod_id_hi2lo : OUTPUT;     dtr_id_lo, dtr_id_hi : BIDIR;     dtr_id_hi2lo : OUTPUT;     read_high_zeros, read_low_zeros : BIDIR;     lnk_status : BIDIR;     can_rst : OUTPUT;     dpmem_en_ = UCC; END DEFAULTS;     mod_id_lo = TRI(0,GND);     mod_id_lo = TRI(0,GND);     read_low_zeros = TRI(0,GND);     tread_low_zeros = TRI(0,GND);     tRBLE     addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst;     1,1,8"00000100" =&gt; 0,1,0;     1,1,8"00000100" =&gt; 1,0,0;     1,1,8"00000100" =&gt; 1,0,0;     1,1,8"00000100" =&gt; 1,0,0;     1,1,8"00000100" =&gt; 1,0,0;     1,1,8"00000100" =&gt; 1,1,1;     0,8,8"xxxxxxx" =&gt; 0,0;     context =&gt; 0;     context =&gt; 0;</pre>	
<pre>read, write, lword : INPUT; a[70] : INPUT; addr_ok : INPUT; mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); dtr_id_lo = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"00000100" =&gt; 0,1,0; 1,1,8"00000100" =&gt; 1,0,0; 1,1,8"00000100" =&gt; 1,0,1; 1,1,8"00000100" =&gt; 1,0,1; 1,1,8"00000100" =&gt; 1,1,0; 1,1,8"00000100" =&gt; 1,1,1; 0,8,8"xxxxxxx" =&gt; 0;</pre>	
<pre>a[70] : INPUT; addr_ok : INPUT; mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); mod_id_hi = TRI(0,GND); tread_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000100" =&gt; 0,1,0; 1,1,B"0000100" =&gt; 0,1,0; 1,1,B"00001100" =&gt; 1,0,1; 1,0,B"00001100" =&gt; 1,0,1; 1,0,B"00001100" =&gt; 1,1,1; 0,x,B"xxxxxxx" =&gt; 0,0; trabLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"001xxxx" =&gt; 0;</pre>	
<pre>addr_ok : INPUT; mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_ni = TRI(0,GND); tread_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); Ink_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 1,0,1; 1,1,B"0000100" =&gt; 1,1,0; 1,1,B"0000100" =&gt; 1,1,1; 0,x,B"xxxxxxxx" =&gt; 0,0;</pre>	
<pre>mod_id_lo, mod_id_hi : BIDIR; mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,6ND); dtr_id_lo = TRI(0,6ND); dtr_id_ni = TRI(0,6ND); read_high_zeros = TRI(0,6ND); read_low_zeros = TRI(0,6ND); lnk_status = TRI(0,6ND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000010" =&gt; 1,1,0; 1,1,B"0000010" =&gt; 1,1,0; 1,1,B"0000010" =&gt; 1,1,0; 1,1,B"0000110" =&gt; 1,1,0; 1,1,0; addr_0k, a[70] =&gt; dpmem_en_; 1, B"001xxxxx" =&gt; 0;</pre>	
<pre>mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; ink_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TR1(0,GND); dtr_id_lo = TR1(0,GND); dtr_id_hi = TR1(0,GND); dtr_id_hi = TR1(0,GND); itread_low_zeros = TR1(0,GND); Ink_status = TR1(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"0000000" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000110" =&gt; 1,0,0; 1,1,B"0000110" =&gt; 1,1,1; 0,x,B"xxxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"001xxxxx" =&gt; 0;</pre>	
<pre>mod_id_hi2lo : OUTPUT; dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; ink_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TR1(0,GND); dtr_id_lo = TR1(0,GND); dtr_id_hi = TR1(0,GND); dtr_id_hi = TR1(0,GND); itread_low_zeros = TR1(0,GND); Ink_status = TR1(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"0000000" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000110" =&gt; 1,0,0; 1,1,B"0000110" =&gt; 1,1,1; 0,x,B"xxxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"001xxxxx" =&gt; 0;</pre>	
<pre>dtr_id_lo, dtr_id_hi : BIDIR; dtr_id_hi2lo : OUTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); 1nk_status = TRI(0,GND); 1,1,B"0000000" =&gt; 0,0,1; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000100" =&gt; 1,0,1; 1,0,B"0000110" =&gt; 1,0,0; 1,1,B"0000100" =&gt; 1,1,1; 0,x,B"xxxxxxxx" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"001xxxxx" =&gt; 0;</pre>	
<pre>dtr_id_hi2lo : 0UTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : 0UTPUT; dpmem_en_ : 0UTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); dtr_id_i0 = TRI(0,GND); dtr_id_in = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"0000000" =&gt; 0,0,1; 1,1,8"0000010" =&gt; 0,1,1; 1,1,8"0000010" =&gt; 1,0,6; 1,1,8"0000100" =&gt; 1,0,1; 1,0,8"0000110" =&gt; 1,1,0; 1,1,8"0000110" =&gt; 1,1,1; 0,x,8"xxxxxxxx =&gt; 0,0,0; END TABLE; addr_ok, a[70] =&gt; dpmem_en_; 1, B"001xxxxx" =&gt; 0;</pre>	
<pre>dtr_id_hi2lo : 0UTPUT; read_high_zeros, read_low_zeros : BIDIR; lnk_status : BIDIR; can_rst : 0UTPUT; dpmem_en_ : 0UTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"0000000" =&gt; 0,0,1; 1,1,8"0000010" =&gt; 0,1,1; 1,1,8"0000010" =&gt; 1,0,6; 1,1,8"0000010" =&gt; 1,0,1; 1,0,8"0000110" =&gt; 1,1,0; 1,1,8"0000110" =&gt; 1,1,1; 0,x,8"xxxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"001xxxxx" =&gt; 0;</pre>	
<pre>Ink_status : BIDIR; can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); Ink_status = TRI(0,GND); Ink_status = TRI(0,GND); 1,1,8"0000000" =&gt; 0,0,1; 1,1,8"00000010" =&gt; 0,1,0; 1,1,8"0000010" =&gt; 0,1,1; 1,1,8"0000010" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,1,0; 1,1,8"0000100" =&gt; 1,1,1; 0,8"0000100" =&gt; 1,1,1; 0,8"0000100" =&gt; 1,1,1; 0,8"0000100" =&gt; 1,1,1; 1,0,8"0000100" =&gt; 1,1,1; 1,0,8"0000100" =&gt; 1,1,1; 0,x,8"xxxxxxx" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"001xxxxx" =&gt; 0;</pre>	
<pre>can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = VCC; END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); Ink_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000010" =&gt; 0,0,1; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000010" =&gt; 1,0,1; 1,0,B"0000110" =&gt; 1,1,1; 0,x,B"xxxxxxxx =&gt; 0,0;</pre>	
<pre>can_rst : OUTPUT; dpmem_en_ : OUTPUT; ) BEGIN DEFAULTS dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000000" =&gt; 0,0,1; 1,1,B"0000010" =&gt; 0,1,0; 1,1,B"0000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 0,1,1; 1,1,B"0000010" =&gt; 1,0,0; 1,1,B"0000100" =&gt; 1,0,0; 1,1,B"0000100" =&gt; 1,1,1; 0,x,B"xxxxxxxx" =&gt; 0,0;</pre>	
<pre>dpmem_en</pre>	
<pre>) BEGIN DEFAULTS     dpmem_en_ = UCC; END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); Ink_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000000" =&gt; 0,0,1; 1,1,B"00000100" =&gt; 0,1,0; 1,1,B"00000100" =&gt; 1,0,0; 1,1,B"0000110" =&gt; 1,0,1; 1,0,B"0000110" =&gt; 1,1,1; 0,x,B"xxxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"0001xxxxx" =&gt; 0;</pre>	
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<pre>END DEFAULTS; mod_id_lo = TRI(0,GND); mod_id_hi = TRI(0,GND); dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); Ink_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"00000000" =&gt; 0,0,1; 1,1,8"00000000" =&gt; 0,1,0; 1,1,8"0000010" =&gt; 0,1,0; 1,1,8"0000010" =&gt; 0,1,1; 1,1,8"00000100" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,0,1; 1,0,8"0000100" =&gt; 1,1,0; 1,1,8"0000110" =&gt; 1,1,1; 0,x,8"xxxxxxx" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"0001xxxxx" =&gt; 0;</pre>	
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<pre>dtr_id_lo = TRI(0,GND); dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"0000000" =&gt; 0,0,1; 1,1,8"0000010" =&gt; 0,1,0; 1,1,8"0000010" =&gt; 0,1,1; 1,1,8"00000100" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,0,1; 1,0,8"0000100" =&gt; 1,1,1; 1,0,8"00001100" =&gt; 1,1,1; 8,x,8"xxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"0001xxxxx" =&gt; 0;</pre>	
<pre>dtr_id_hi = TRI(0,GND); read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"00000000" =&gt; 0,0,1; 1,1,8"00000100" =&gt; 0,1,0; 1,1,8"00000100" =&gt; 0,1,1; 1,1,8"00000100" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,0,1; 1,0,8"0000100" =&gt; 1,0,1; 1,0,8"0000100" =&gt; 1,1,1; 0,x,8"xxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"0001xxxxx" =&gt; 0;</pre>	
<pre>read_high_zeros = TRI(0,GND); read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,8"00000000" =&gt; 0,0,1; 1,1,8"00000100" =&gt; 0,1,1; 1,1,8"00000100" =&gt; 0,1,1; 1,1,8"0000110" =&gt; 1,0,0; 1,1,8"0000100" =&gt; 1,0,1; 1,0,8"00001010" =&gt; 1,1,1; 0,x,8"xxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, 8"0001xxxxx" =&gt; 0;</pre>	
<pre>read_low_zeros = TRI(0,GND); lnk_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000000" =&gt; 0,0,1; 1,1,B"00000010" =&gt; 0,1,0; 1,1,B"00000100" =&gt; 0,1,1; 1,1,B"0000110" =&gt; 1,0,0; 1,1,B"00001000" =&gt; 1,0,1; 1,0,B"0000100" =&gt; 1,1,1; 0,x,B"xxxxxxxx" =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"0001xxxxx" =&gt; 0;</pre>	
<pre>Ink_status = TRI(0,GND); TABLE addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000000" =&gt; 0,0,1; 1,1,B"00000010" =&gt; 0,1,0; 1,1,B"00000100" =&gt; 0,1,1; 1,1,B"0000110" =&gt; 1,0,0; 1,1,B"00001000" =&gt; 1,0,1; 1,0,B"0000100" =&gt; 1,1,0; 1,1,B"00001100" =&gt; 1,1,1; 0,x,B"xxxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"0001xxxxx" =&gt; 0;</pre>	
TABLE         addr_ok, read, a[70]       => dtr_id_hi2lo, mod_id_hi2lo, can_rst;         1,1,B"00000000"       => 0,0,1;         1,1,B"00000010"       => 0,1,0;         1,1,B"00000100"       => 0,1,1;         1,1,B"00000100"       => 0,1,1;         1,1,B"00001100"       => 1,0,0;         1,1,B"00001000"       => 1,0,1;         1,6,B"00001100"       => 1,1,0;         1,1,B"00001100"       => 1,1,1;         0,x,B"xxxxxxxx"       => 0,0,0;         END TABLE;       TABLE         addr_ok, a[70]       => dpmem_en_;         1,       B"001xxxxx"       => 0;	
<pre>addr_ok, read, a[70] =&gt; dtr_id_hi2lo, mod_id_hi2lo, can_rst; 1,1,B"00000000" =&gt; 0,0,1; 1,1,B"00000010" =&gt; 0,1,0; 1,1,B"00000100" =&gt; 0,1,1; 1,1,B"00000100" =&gt; 1,0,0; 1,1,B"00001000" =&gt; 1,0,1; 1,0,B"00001010" =&gt; 1,1,1; 0,x,B"xxxxxxx =&gt; 0,0,0; END TABLE; TABLE addr_ok, a[70] =&gt; dpmem_en_; 1, B"0001xxxxx" =&gt; 0;</pre>	
1,1,B"90900000" => 0,0,1; 1,1,B"90900010" => 0,1,0; 1,1,B"90900100" => 0,1,1; 1,1,B"90900100" => 1,0,0; 1,1,B"90901000" => 1,0,1; 1,0,B"90901010" => 1,1,0; 1,1,B"90901100" => 1,1,1; 0,x,B"xxxxxxx => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B"901xxxxx" => 0;	
1,1,8"90900010" => 0,1,0; 1,1,8"90900100" => 0,1,1; 1,1,8"90900100" => 1,0,0; 1,1,8"90901000" => 1,0,1; 1,0,8"90901010" => 1,1,0; 1,1,8"90901100" => 1,1,1; 0,x,8"xxxxxxx => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, 8"001xxxxx" => 0;	
1,1,B"0000100" => 0,1,1; 1,1,B"0000100" => 1,0,0; 1,1,B"00001000" => 1,0,1; 1,0,B"00001010" => 1,1,0; 1,1,B"0001100" => 1,1,1; 0,x,B"xxxxxxx" => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B"001xxxxx" => 0;	
1,1,B"00000110" => 1,0,0; 1,1,B"00001000" => 1,0,1; 1,0,B"00001010" => 1,1,0; 1,1,B"00001100" => 1,1,1; 0,x,B"xxxxxxx" => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B"001xxxxx" => 0;	
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1,0,B"00001010" => 1,1,0; 1,1,B"00001100" => 1,1,1; 0,x,B"xxxxxxx" => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B"001xxxxx" => 0;	
1,1,B"00001100" => 1,1,1; 0,x,B"xxxxxxx" => 0,0,0; END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B"001xxxxx" => 0;	
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END TABLE; TABLE addr_ok, a[70] => dpmem_en_; 1, B''001xxxxx'' => 0;	
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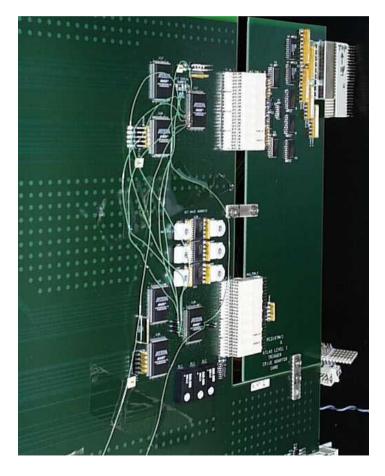
#### Now where are we.?

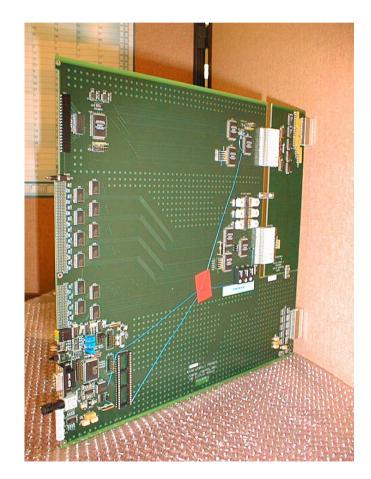
Binary decoded addressing has been implemented and all registers work OK.

Takes only 1 - 2 hours to modify and program CPLD's.



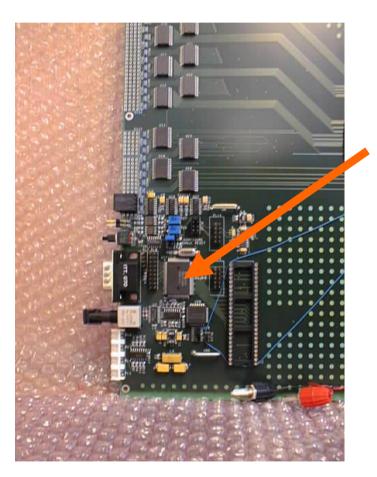
## **The Improvement**





## **Further Testing Problems**

- Can not download to the CAN micro on the "old board".
- New board can obtain connection, continue tests with new board, maybe.!

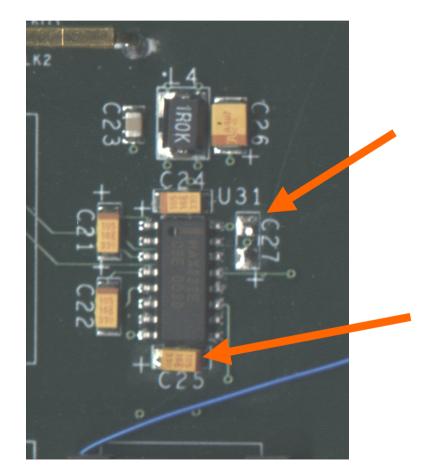


# **Further Testing Problems**

- Microprocessor responds correctly to serial commands.
- MAX232 was found to be dead, not giving output.
- Capacitors C27 and C25 were placed on the schematic the wrong. Pulling down internally generated voltage supply.

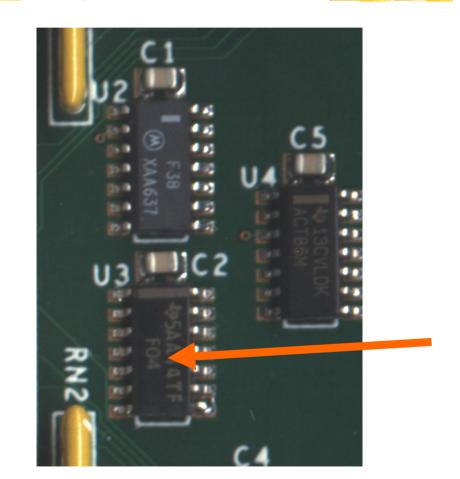
## **Further Testing Problems**

- Capacitors around the wrong way.!
- C27 de-couple +5V on board. Bang.!!
- C25 de-couple internal 232 supply.



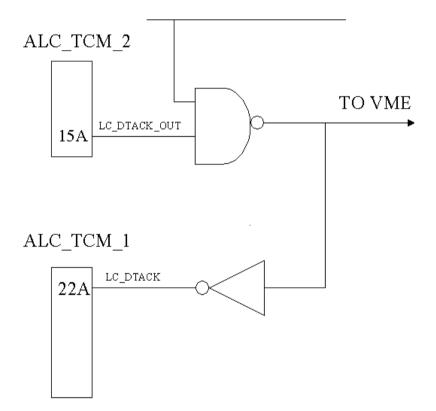
# **Future ALC Designs**

- No Need for U3 to feed back DTACK signal.
- It is generated onboard.!



# **ALC Design Considerations**

- Circuit not required.
  No need to feed signal back to ALC\_TCM\_1.
- DTACK is generated on board.



# Finally

PECL Distribution, OK.CAN Buss download, OK

Left to test:-

- CAN controller.
- Works in the new crate.

#### **Time Scales**

Do We get the other boards populated?
CAN Buss Interface working?
??????